

TFT-LCD Module

SPECIFICATION

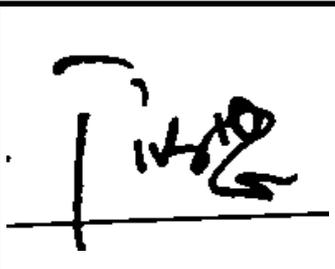
Customer: _____
Model Name: VI101EI342
SPEC NO.: _____
Date: 2021.05.06
Version: V01

Preliminary Specification

Final Specification

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
		



Record of Revision

Toroson Group copyright 2021
All right reserved, Copying forbidden.

Version	Revise Date	Page	Content

Contents

1. FEATURES-----	4
2. GENERAL SPECIFICATIONS-----	4
3. PIN DESCRIPTION-----	5
3.1 Golden finger-----	5
3.2 PIN assignment-----	5
3.3 Advice circuit for customer system-----	8
4. ABSOLUTE MAXIMUM RATING-----	10
5. DC CHARCTERISTICS-----	11
5.1 Parameter-----	11
5.2 Current Consumption-----	11
5.3 Power Sequence-----	11
6. AC CHARCTERISTICS-----	13
6.1 Data Input Format-----	13
6.2 Parallel RGB Input Timing Table-----	13
6.3 AC Electrical Characteristic-----	14
7. OPTICAL CHARACTERISTIC-----	16
7.1 Optical Specification-----	16
7.2 Basic measure condition-----	16
8. QUALITY ASSURANCE-----	18
9. HANDING CAUTIONS-----	19
9.1 ESD (Electrical Static Discharge) Strategy-----	19
9.2 Environment-----	19
9.3 Others-----	19
10. MECHANICAL DRAWING-----	21
11. PACKAGE DRAWING-----	22

1. FEATURES

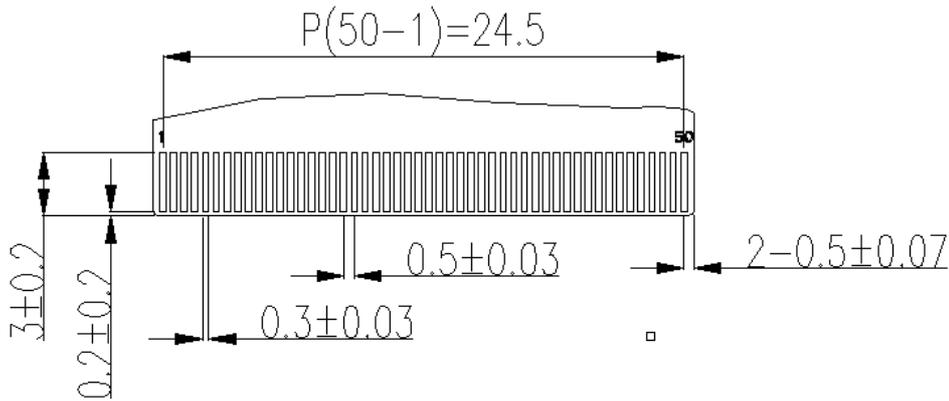
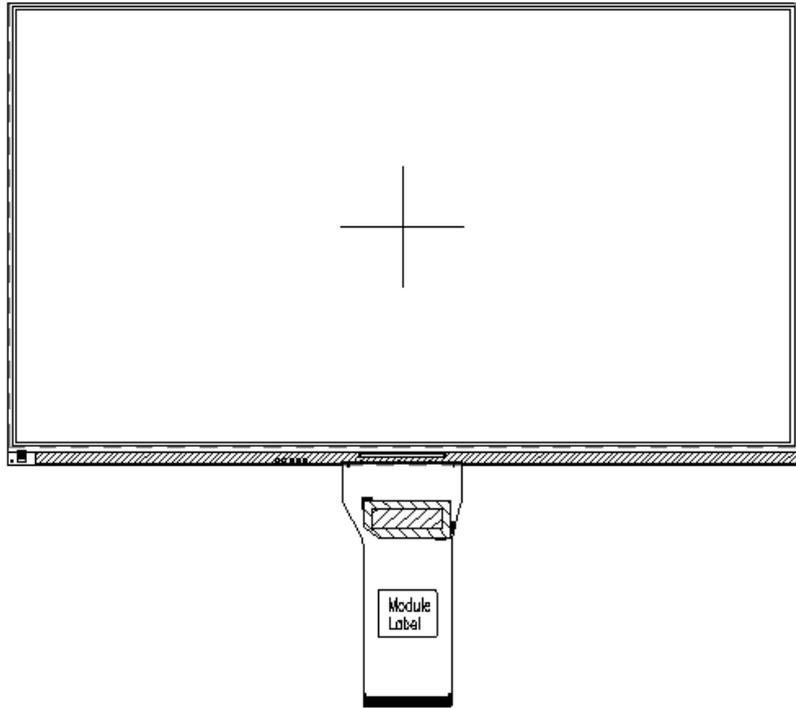
VI101EI342 is a transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This panel has a 10.1 inches diagonally measured active display area with 1024 x 600 resolution. This product is composed of a TFT LCD panel, Polarizers, driver ICs and FPC.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size	10.1	inch
Display Type	Transmissive, a-Si	-
Active Area (HxV)	222.72 (H) x 125.28 (V)	mm
Number of Dots (HxV)	1024 x RGB x 600	dot
Pixel Pitch(HxV)	0.2175 x 0.2088	mm
Color Arrangement	RGB Stripe	-
Color Numbers	16.7 M	-
Outline Dimension (HxVxD)	235 (H) x 143 (V) x 5.0(D)	mm
NTSC (CIE1931) (Under CF on C light)	50 (Typ.)	%
Response Time	≤35	ms
Viewing Angle (Light On) (R/U/L/D)	CR ≥ 10 @ R/L/U/D(80°/80°/80°/80°) (Typ.)	
Surface Treatment	HC	
Contrast Ratio (Light On)	800:1 (Typ)	
Operation Temperature	-20~70	°C
Storage Temperature	-20~70	°C
Interface	RGB(TTL)	
Weight	85.4	g
IC	ILI6150 & ILI5120	

3. Pin Description

3.1 Golden finger PIN pitch = 0.5mm



3.2 PIN assignment

No	Symbol	I/O	Function	Remark
1	LED+	P	LED Anode	
2	LED+	P	LED Anode	
3	LED-	P	LED Cathode	
4	LED-	P	LED Cathode	
5	GND	P	Ground	

SPEC NO.:VI101EI342

Date: 2021/05/06

6	VCOM	P	Common Voltage	
7	VDD	P	Power Voltage for digital circuit	
8	MODE	I	DE/SYNC mode select	Note 1
9	DE	I	Data input enable	
10	VSYNC	I	Vertical Sync Input	
11	HSYNC	I	Horizontal Sync Input	
12	B7	I	Blue data(MSB)	
13	B6	I	Blue data	
14	B5	I	Blue data	
15	B4	I	Blue data	
16	B3	I	Blue data	
17	B2	I	Blue data	
18	B1	I	Blue data	
19	B0	I	Blue data(LSB)	
20	G7	I	Green data (MSB)	
21	G6	I	Green data	
22	G5	I	Green data	
23	G4	I	Green data	
24	G3	I	Green data	
25	G2	I	Green data	
26	G1	I	Green data	
27	G0	I	Green data(LSB)	
28	R7	I	Red data (MSB)	
29	R6	I	Red data	
30	R5	I	Red data	
31	R4	I	Red data	
32	R3	I	Red data	
33	R2	I	Red data	
34	R1	I	Red data	
35	R0	I	Red data(LSB)	
36	GND	P	Ground	
37	DCLK	I	Date CLK	
38	GND	P	Ground	
39	L/R	I	Right/ left selection	Note 2
40	U/D	I	Up/down selection	Note 2
41	VGH	P	Gate ON voltage	
42	VGL	P	Gate OFF voltage	
43	AVDD	P	Power for Analog circuit	

44	RESET	I	Global reset pin.	Note 3
45	NC	-	No connection	
46	VCOM	P	Common voltage	
47	DITHER	I	Dithering function	Note 4
48	GND	P	Ground	
49	NC	-	No connection	
50	NC	-	No connection	

I: input, O: output, P: power

Note 1: DE/SYNC mode select. Normally pull high.

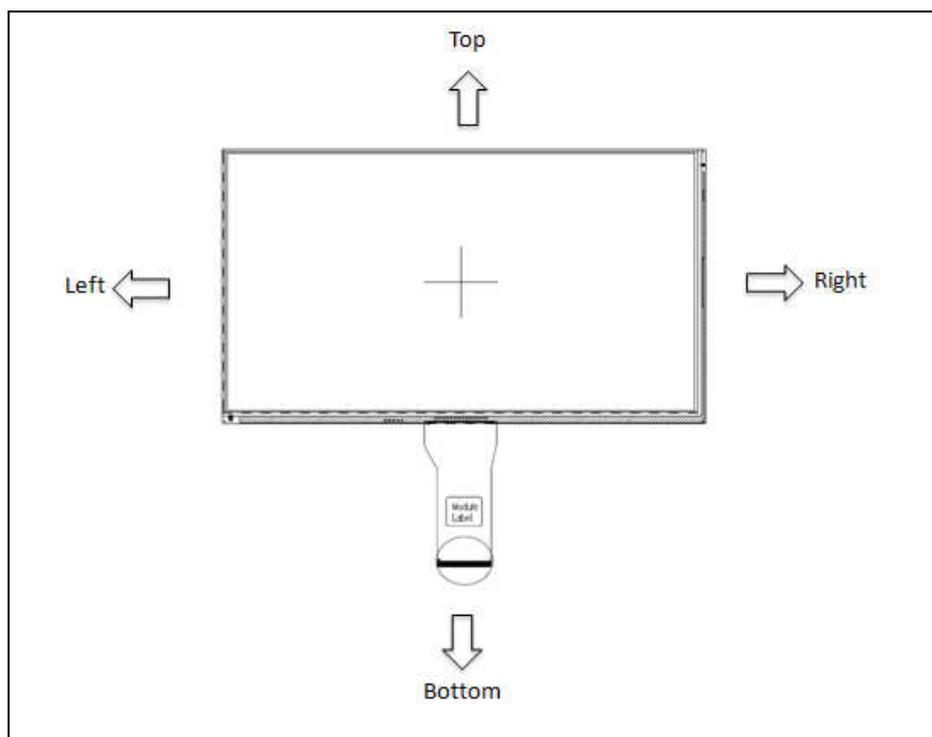
H: DE mode.

L: HS/VS mode.

Note 2: Selection of scanning mode

Setting of scan control input		Scanning direction
U/D	L/R	
GND	VDD	Up to down, left to right
VDD	GND	Down to up, right to left
GND	GND	Up to down, right to left
VDD	VDD	Down to up, left to right

Definition of scanning direction .Refer to the figure as below



Note 3: Global reset pin. Active Low to enter reset State. Suggest to connecting with an RC Reset circuit for stability. Normally pull high.

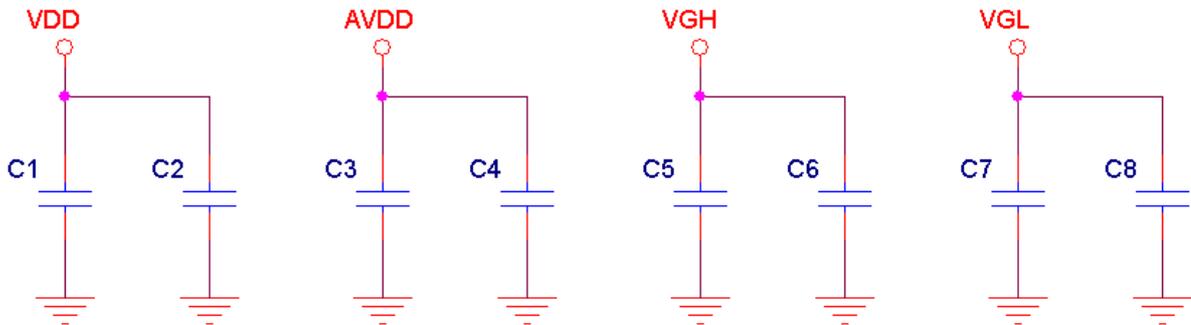
Note4: Dithering function Enable control. Normally pull high.

DITHB="1", Disable internal dithering function. For 18bit RGB interface,
Connect two LSB bits of all the R/G/B data buses to GND.

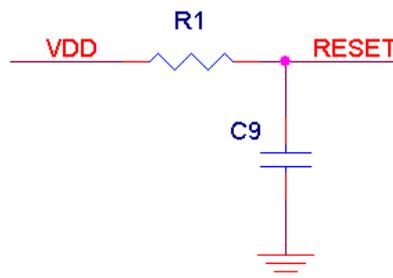
DITHB="0", Enable internal dithering function, For TTL 24bit parallel RGB image
Data enable

3.3 Advice circuit for customer system

3.3.1 Power PIN: AVDD/VDD/VGH/VGL

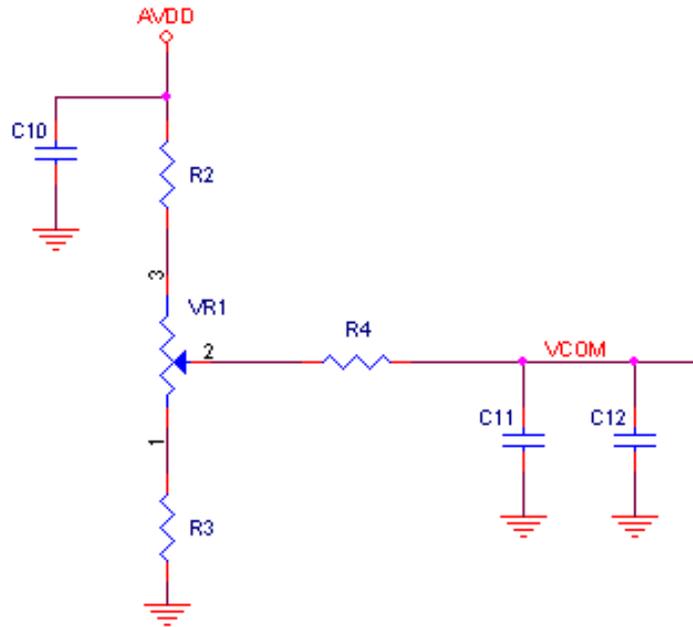


3.3.2 Control PIN: RESET



3.3.3 VCOM

Typical VCOM is only a reference value, it must be optimized according to each LCM. Be sure to use VR;



3.3.4 VCOM

Location	Description
C1,C11	10uF,X5R,10V
C2,C12	100nF,X5R,10V
C3,C7	10uF,X5R,25V
C4,C8	100nF,X5R,25V
C5	10uF,X5R,50V
C6	100nF,X5R,50V
C9	1uF,X5R,10V
C10	1uF,X5R,25V
R1	10Kohm,1%
R2	12Kohm,1%
R3	10Kohm,1%
R4	0ohm,1%
VR1	10Kohm,1%

4. ABSOLUTE MAXIMUM RATING

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	3.6	V	
	AVDD	-0.3	15	V	
	VGH	-0.3	30	V	
	VGL	-15	0.3	V	
Storage temperature	Tstg	-30	+80	°C	
Operating Temperature	Topr	-20	+70	°C	

Note:

- (1) All of the voltages listed above are with respect to GND= 0V
- (2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

4.1 Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED backlight	V _L	8.4	9.0	10.5	V	Note 1
Current for LED backlight	I _L	-	240	-	mA	
LED life time	-	20,000	-	-	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25°C and IL=240mA

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=240mA. The LED lifetime could be decreased if operating IL is larger than 240mA.

5. DC CHARACTERISTICS

5.1 Parameter

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Power supply voltage	VDD	3.0	3.3	3.6	V	
	AVDD	12	12.2	12.4	V	
	VGH	20	22	24	V	
	VGL	-11	-10	-9	V	
Input signal voltage	VCOM	4.39	5.39	6.39	V	
Logic high level input voltage	VIH	0.7xVDD	-	VDD	V	Note 1
Logic low level input voltage	VIL	VSS	-	0.3xVDD	V	

(Ta = 25 ± 2°C)

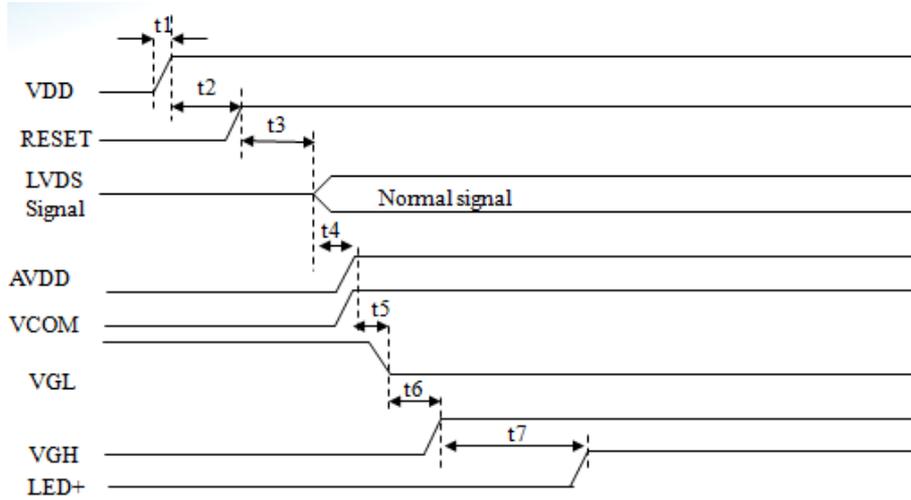
Note 1: Including signal: MODE、DE、VSYNC、HSYNC、DCLK、U/D、L/R、RESET、DITHER.

5.2 Current Consumption

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Current for Driver	IVDD	10	15	20	mA	VDD=3.3V
	IAVDD	8	45	65	mA	AVDD=12.2V
	IVGH	0.1	0.6	2	mA	VGH=22V
	IVGL	0.1	0.6	2	mA	VGL=-10V

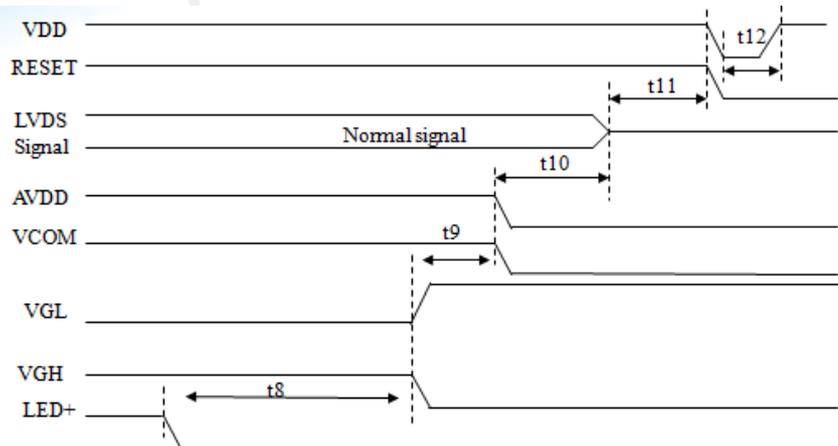
5.3 Power Sequence

Power on



Symbol	SPEC			Unit
	Min.	Typ.	Max.	
t1	1	10	20	ms
t2	1	10(RC Delay)	12	ms
t3	30	50	100	ms
t4	0.1	5	20	ms
t5	20	70	120	ms
t6	40	90	140	ms
t7	150	170	200	ms

Power off

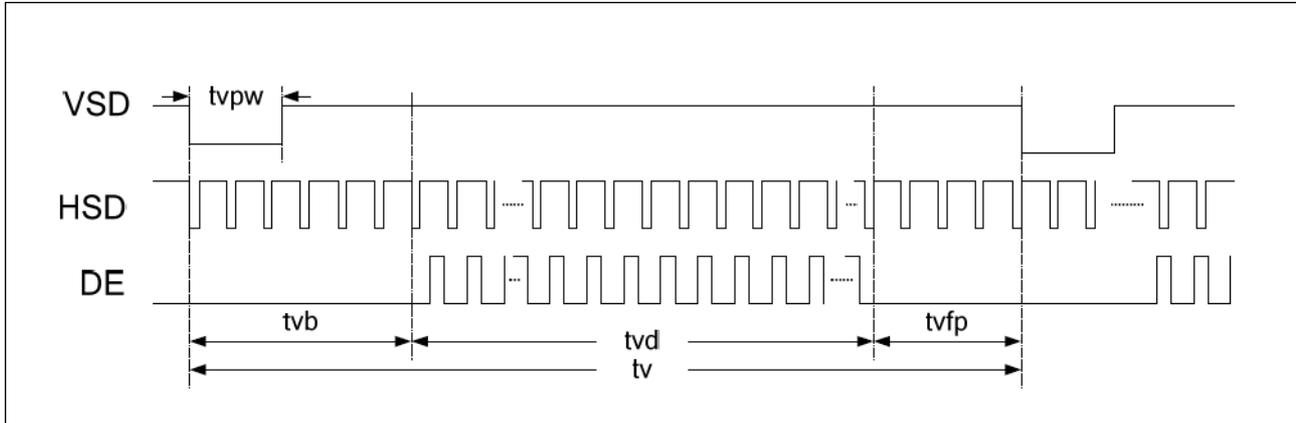


Symbol	SPEC			Unit
	Min.	Typ.	Max.	
t8	120	150	200	ms
t9	50	100	200	ms
t10	1	10	20	ms
t11	0.1	10	100	ms
t12	500	-	-	ms

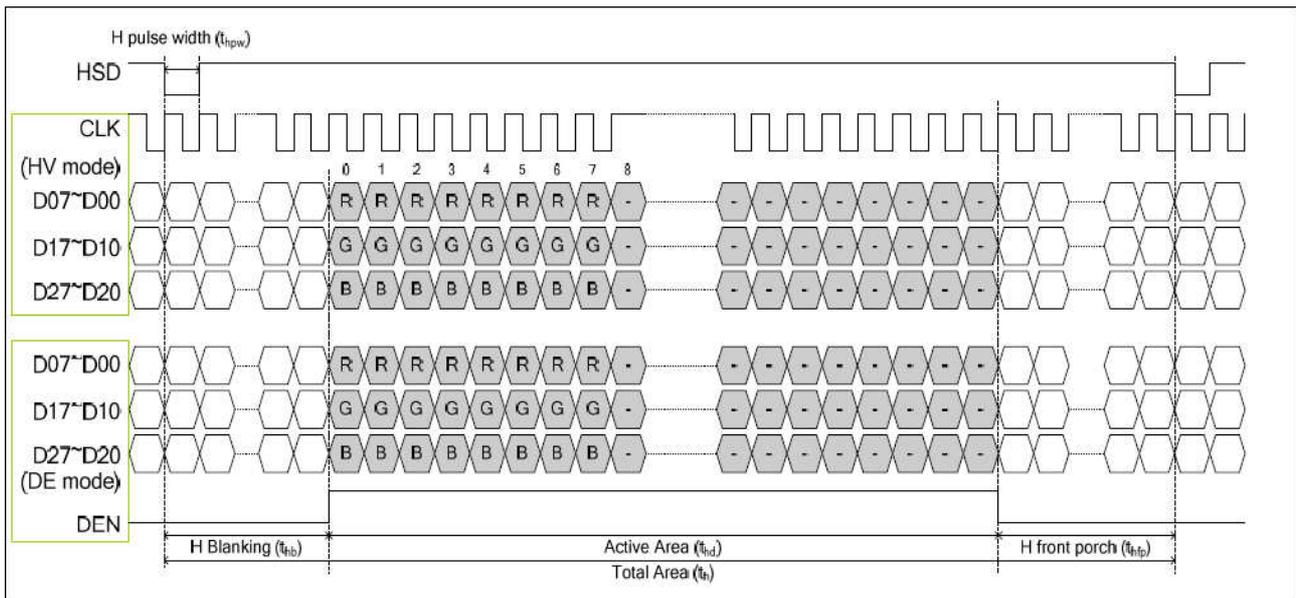
6. AC CHARACTERISTICS

6.1 Data input format

Vertical input Timing



Horizontal input Timing



6.2 Parallel RGB input timing table

Parallel RGB input timing table

DE mode

Parallel	Symbol	Vaule			Unit
		Min	Typ	Max	
DCLK Frequency Frame rate=60Hz	fclk	42.5	51.2	67.2	MHz
Horizontal display area	thd	1024			DCLK
HSYNC period time	thpw	1164	1344	1400	DCLK
HSYNC blanking	thb+thfp	140	320	376	DCLK

SPEC NO.: VI101EI342

Date: 2021/05/06

Vertical display area	tvd	600			H
VSYNC period time	tpw	610	635	800	H
VSYNC blanking	tvb+tvfp	10	35	200	H

HV mode

a. Horizontal input timing

Parallel	Symbol	Vaule			Unit
		Min	Typ	Max	
Horizontal display area	thd	1024			
DCLK Frequency Frame rate=60Hz	fclk	44.9	51.2	63	MHz
1 Horizontal Line	th	1200	1344	1400	DCLK
HSYNC pulse width	thpw	Min	1		DCLK
		Typ	-		
		Max	140		
HSYNC period time	thpw	160	160	160	
HSYNC blanking	thb+thfp	16	160	216	

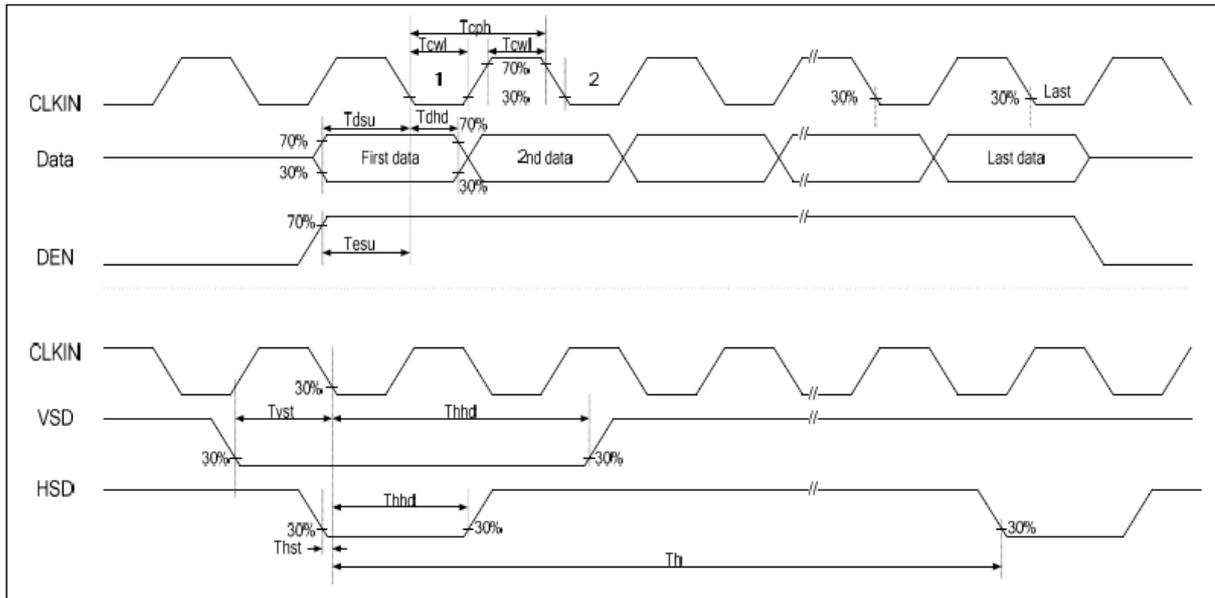
b. Vertical input timing

Parallel	Symbol	Vaule			Unit
		Min	Typ	Max	
Vertical display area	tvd	600			H
VSYNC period time	tv	624	635	760	H
VSYNC pulse width	tpw	1	-	20	H
VSYNC blanking	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

6.3 AC Electrical characteristic

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
HS setup time	T_{hst}	5	-	-	ns
HS hold time	T_{hhd}	5	-	-	ns
VS setup time	T_{vst}	5	-	-	ns
VS hold time	T_{vhd}	5	-	-	ns
Data setup time	T_{dsu}	5	-	-	ns
Data hold time	T_{dhd}	5	-	-	ns
DE setup time	T_{esu}	5	-	-	ns
DE hold time	T_{ehd}	5	-	-	ns

VDD Power On Slew Rate	T_{POR}	-	-	20	ms
CLKIN cycle time	T_{cph}	14	-	-	ns
CLKIN pulse duty	T_{cwh}	40	50	60	%
Output stable time	T_{sst}	-	-	3	us



TOROSON

7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

Ta=25°C

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (Cr ≥ 10)	θ_L	$\Phi = 180^\circ$ (9 o'clock)	75	80	-	degree	Note7- 1
	θ_R	$\Phi = 0^\circ$ (3 o'clock)	75	80	-		
	θ_T	$\Phi = 90^\circ$ (12 o'clock)	75	80	-		
	θ_B	$\Phi = 270^\circ$ (6 o'clock)	75	80	-		
Response time	T_{ON} + T_{OFF}	Normal $\theta = \Phi = 0^\circ$	-	25	35	msec	Note 7-2
Contrast ratio	C_R		600	800	-	-	Note7- 4
Color chromaticity	W_X		0.26	0.31	0.36	-	Note 7-5
	W_Y		0.28	0.33	0.38	-	
Luminance	L		300	350	-	cd/m ²	Note7-6
Luminance uniformity	Y_U		70	75	-	%	

7.2 Basic measure condition

(1) Driving voltage

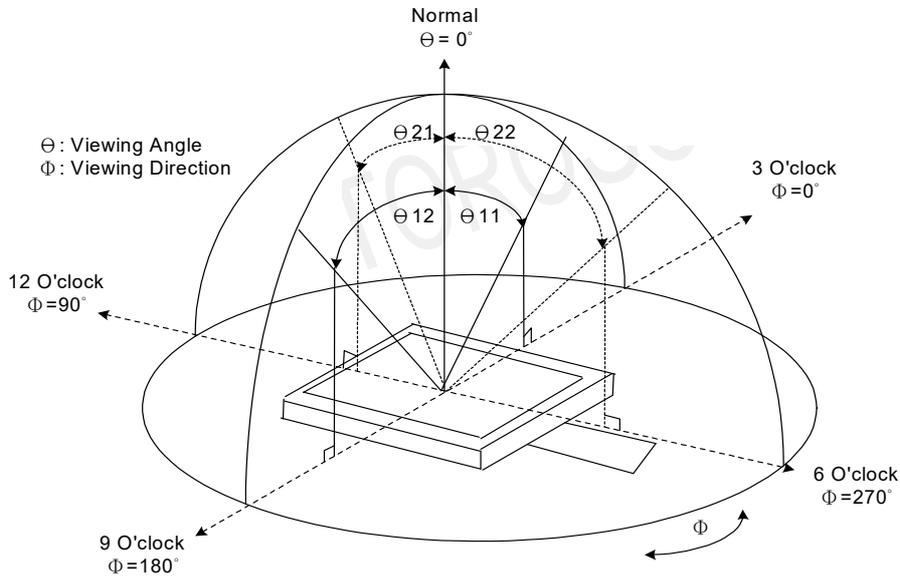
Based on item 5. DC CHARACTERISTICS and 6. AC CHARACTERISTICS

(2) Ambient temperature: Ta=25°C

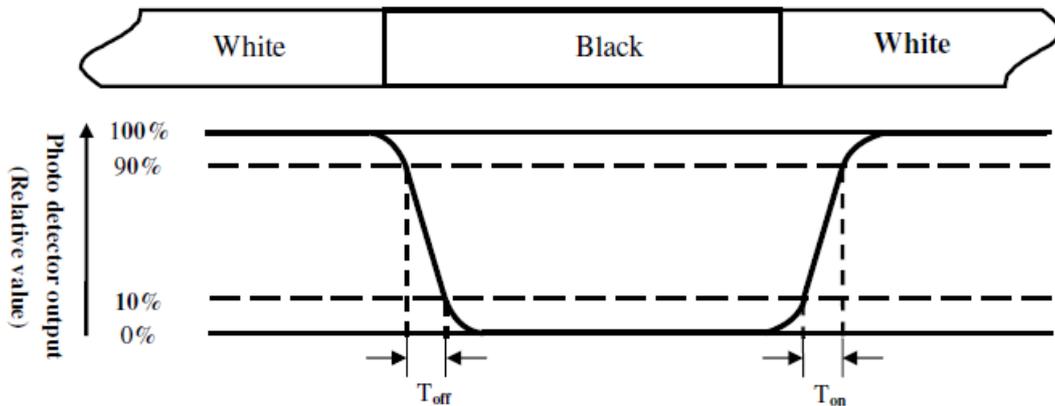
(3) Testing point: measure in the display center point and the test angle $\theta=0^\circ$

(4) Testing Facility: Environmental illumination: ≤ 1 Lux

Note 7-1: Viewing angle diagrams



Note 7-2: Response time



Note 7-3: Transmittance

The transmittance is measured on INX stabilized backlight.

Note 7-4: Contrast ratio

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \text{White} / \text{Black}$$

Note 7-5 Chromaticity

The chromaticity is measured in CIE 1931 at the center point of CF on C Light Source.

8. QUALITY ASSURANCE

No.	Test Items	Test Condition	Note
1	High Temperature Storage	70°C, 240hrs	Note 1, 2
2	Low Temperature Storage	-20°C, 240hrs	Note 1, 2
3	High Temperature Operation	70°C, 240hrs	Note 1, 2
4	Low Temperature Operation	-20°C, 240hrs	Note 1, 2
5	High Temperature and High Humidity Storage	60°C, 90%RH, 240hrs	Note 1, 2
6	Thermal Shock	-20°C/0.5h ~ +70°C/0.5h for a total 100 cycles	Note 1, 2
7	Electro Static Discharge	C=150pF,R=330Ω, 5point/panel Air:±4Kv, 5times	Note 2
8	Package Drop Test	Height:60cm,1 corner,3 edges,6 surfaces	Note 2

Note 1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

Note 2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

9. HANDLING CAUTIONS

9.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

- (1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.
- (2) The machine and working table for the panel should have ESD protection strategy.
- (3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.
- (4) In the process of assemble module, shield case should connect to the ground.

9.2 Environment

- (1) Working environment of the panel should be in the clean room.
- (2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

9.3 Others

- (1) Turn off the power supply before connecting and disconnecting signal input cable.
- (2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.
- (3) Water drop on the surface or condensation as panel power on will corrode panel electrode.
- (4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
- (5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.
- (6) Unpacking (Hard Box) in order to prevent open cells broken:
 - [6.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.
 - [6.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.
 - [6.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below.
 - [6.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.
 - [6.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.
 - [6.3.3] Do not press the surface of an open cell in a hard box.
 - [6.3.4] Do not pull X-board when an open cell placed in a hard box.

(7) Handling – In order to prevent open cells, COFs , and components damaged:

[7.1] The forced displacement between open cells and X-board may cause a COF damaged.

Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

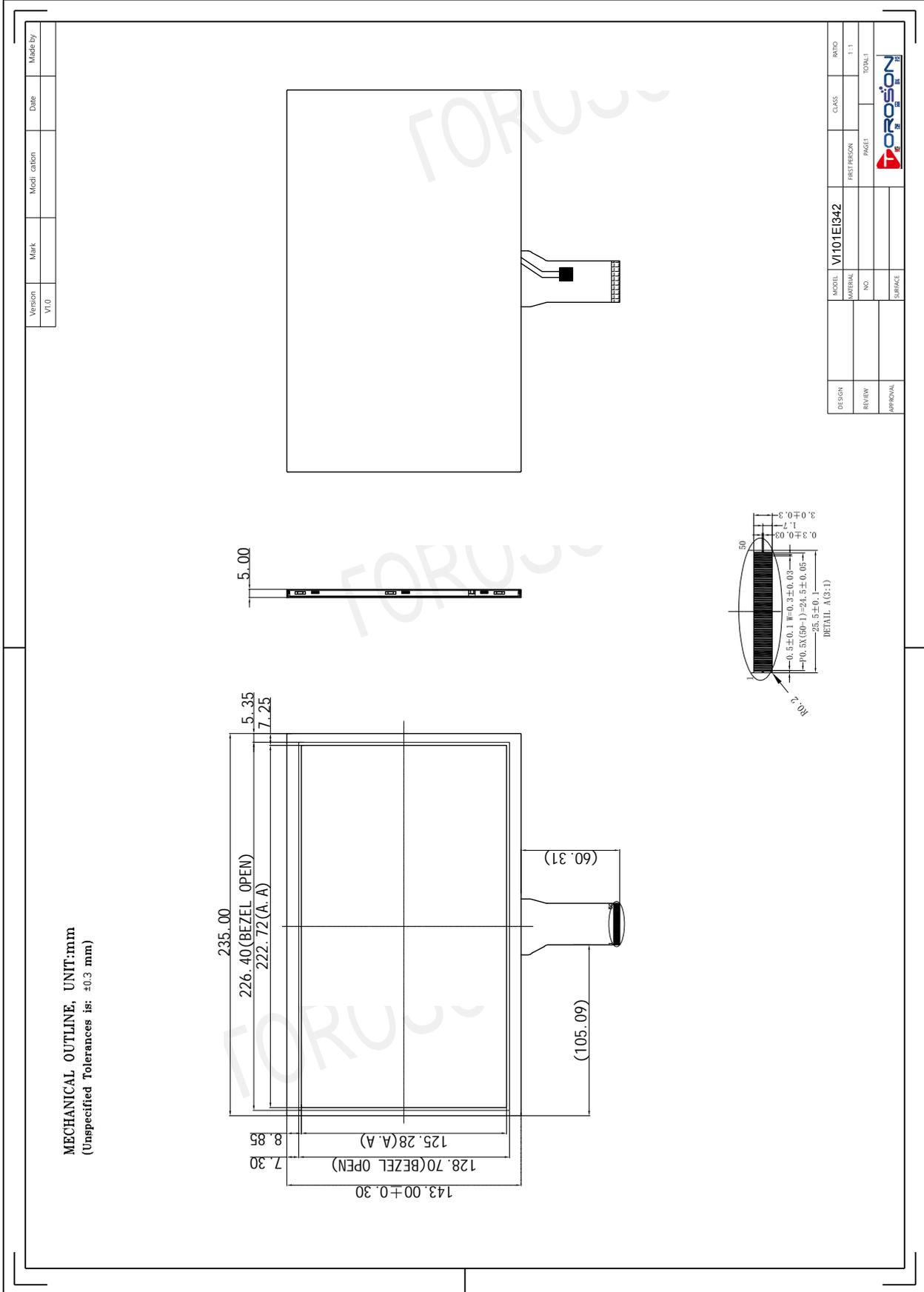
[7.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[7.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[7.4] Handle open cells one by one.

(8) Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

7. Mechanical Drawing



11. Packaging Drawing

TBD

TOROSON

TOROSON

TOROSON