Doc. Number: V0

■Tentative Specification(DR2)
□ Preliminary Specification
□ Approval Specification

MODEL NO.: JE070IA
SUFFIX: 18J

Customer:
APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note :

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Henry Chien	Annie Lu	Tony Wang

CONTENTS

REVISION HISTORY

Version	Date	Page	Description
V0	2018/07/31	All	Pre-Spec Ver.0.0 was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

JE070IA-18J is a 7” (7” diagonal) TFT Liquid Crystal Display FOG without LED Backlight unit and with 60 pins TTL interface. This FOG supports 800 x 480 WVGA mode.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	7” diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	800 x R.G.B. x 480	pixel	-
Pixel Pitch	0.1905 (H) x 0.1905 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216 (8bit color depth)	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	HC	-	-
Transmittance	4.8	%	Typ.
Power Consumption	615	*mW*	(1)

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VDD = 3.3 V, f = 60 Hz, and Ta = 25 ± 2 ºC, whereas white pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
FOG Shipping Size	Horizontal (H)	159.9	160.2	160.5	mm	(1)
	Vertical (V)	101.4	101.7	102	mm	
	Thickness (T)	1.17	1.27	1.37	mm	
CF Polarizer	Horizontal	154.5	154.8	155.1	mm	(1)
	Vertical	93.7	94	94.3	mm	
TFT Polarizer	Horizontal	159.3	159.6	159.9	mm	(1)
	Vertical	97.24	97.54	97.84	mm	
Active Area	Horizontal		152.4		mm	
	Vertical		91.44		mm	
Weight		42	44	46	g	

Note (1) Please refer to the attached drawings.

JE070IA-18J-FOG-B -drawing0713.pdf

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Voltage	V_{DD}	-0.5	5	V	(5)
Storage Temperature	T_{ST}	Ta=-40	Ta=90	ºC	(1)(2)(3)(4)
Operating Ambient Temperature	T_{OP}	Ta=-30	Tp=85	ºC	(1)(2)(3)(4)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) Ta = Ambient Temperature, Tp = Panel Surface Temperature.

Note (3) This rating applies to all parts of the module and should not be exceeded.

Note (4) If the product were used out of the operation and storage range, it will have quality issue

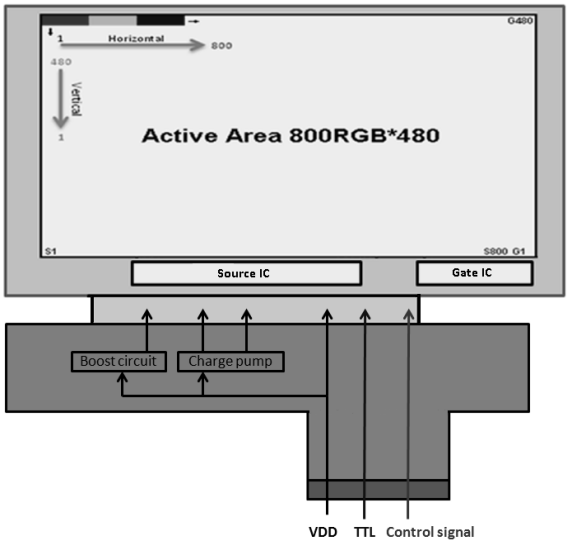
Note (5) The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

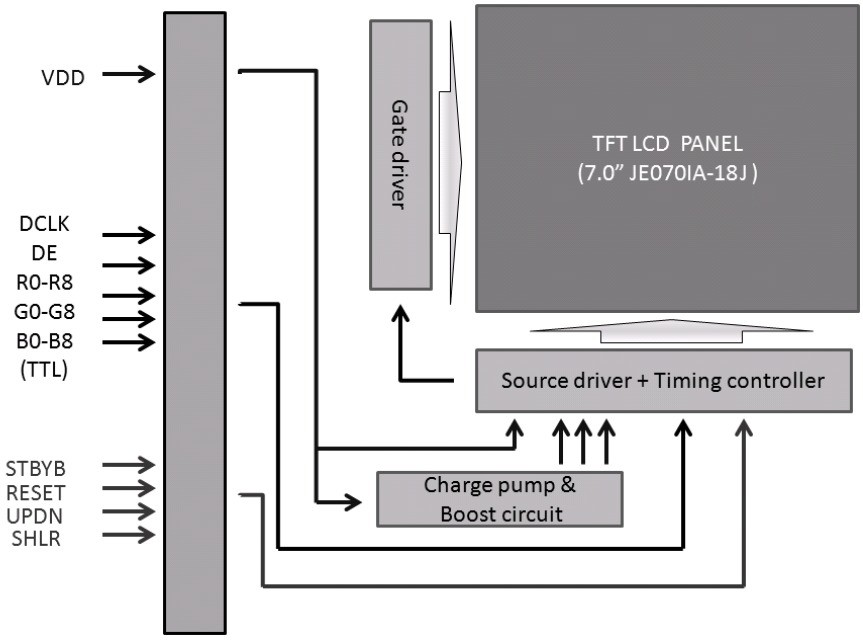
4. ELECTRICAL SPECIFICATIONS

4.1 DESCRIPTION DISPLAY ELECTRONICS

The display module comes with an 8 bits TTL interface. The display's data and synchronization signals (DE, CLK,…) , which generates all necessary control signals for the source driver and gate driver. Single VDD voltage inputs are required for display functional operation. Gamma setting adjustment is done by Innolux with default value. Please refer to the block diagram in section 4.2

4.2 BLOCK DIAGRAM





4.3 TYPICAL OPERATION CONDITIONS

Ta=25℃

item	Symbol	Min.	Typ.	Max.	Unit.	Note.
Digital Supply Voltage	VDD	3.1	3.3	3.6	V	
Logic Input Voltage	VIH	0.7VDD	-	VDD	V	
	VIL	GND	-	0.3VDD	V	

4.4 INTERFACE CONNECTIONS

The Connector recommended model is IMSA-12001S-60Y903 manufactured by IRISO.

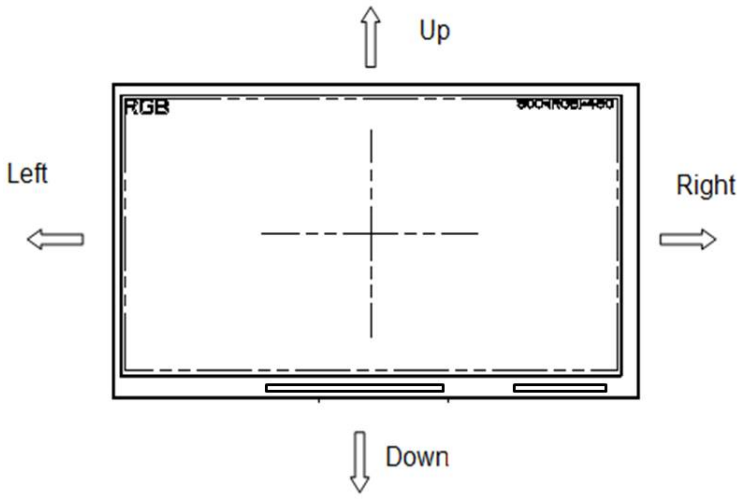
Connector type：IMSA-12001S-60Y903					
PIN NO.	Symbol	I/Opin (I:input, O:output, P:power)	Typical voltage (Volt)		Function
1	GND	P	0.00 V	Power supply	GND
2	NC				Keep floating
3	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
4	R0	I		TTL signal	Red Data (LSB)
5	R1	I		TTL signal	Red Data
6	R2	I		TTL signal	Red Data
7	R3	I		TTL signal	Red Data
8	R4	I		TTL signal	Red Data
9	R5	I		TTL signal	Red Data
10	R6	I		TTL signal	Red Data
11	R7	I		TTL signal	Red Data (MSB)
12	G0	I		TTL signal	Green Data (LSB)
13	G1	I		TTL signal	Green Data
14	G2	I		TTL signal	Green Data
15	G3	I		TTL signal	Green Data
16	G4	I		TTL signal	Green Data
17	G5	I		TTL signal	Green Data
18	G6	I		TTL signal	Green Data
19	G7	I		TTL signal	Green Data (MSB)
20	B0	I		TTL signal	Blue Data (LSB)
21	B1	I		TTL signal	Blue Data
22	B2	I		TTL signal	Blue Data
23	B3	I		TTL signal	Blue Data
24	B4	I		TTL signal	Blue Data
25	B5	I		TTL signal	Blue Data
26	B6	I		TTL signal	Blue Data
27	B7	I		TTL signal	Blue Data (MSB)
28	DCLK	I		TTL signal	Clock signal

29	DE	I		TTL signal	Data Enable
30	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
31	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
32	NC				Keep floating
33	RESET	I	3.3V or 0V	Function	Global reset pin (Default high), active low.
34	STBYB	I	3.3V or 0V	Function	Standby mode setting pin (Default high), active low.
35	SHLR	I	3.3V or 0V	Function	Horizontal scan direction (Default high), Note (1)
36	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
37	UPDN	I	3.3V or 0V	Function	Vertical scan direction (Default high), Note (1)
38	GND	P	0.00 V	Power supply	GND
39	GND	P	0.00 V	Power supply	GND
40	NC				Keep floating
41	NC				Keep floating
42	NC				Keep floating
43	NC				Keep floating
44	NC				Keep floating
45	NC				Keep floating
46	NC				Keep floating
47	NC				Keep floating
48	NC				Keep floating
49	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
50	NC				Keep floating
51	GND	P	0.00 V	Power supply	GND
52	GND	P	0.00 V	Power supply	GND
53	GND	P	0.00 V	Power supply	GND
54	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
55	NC				Keep floating
56	NC				Keep floating
57	VDD	P	3.3 V	Power supply	External main and I/O power supply ; Power 3.3V
58	NC				Keep floating
59	GND	P	0.00 V	Power supply	GND
60	NC				Keep floating

Note (1)

SHLR	UPDN	Data shifting
VDD	VDD	Left→Right，UP→Down(default)
VDD	GND	Left→Right，Down→UP
GND	VDD	Right→Left，UP→Down
GND	GND	Right→Left，Down→UP

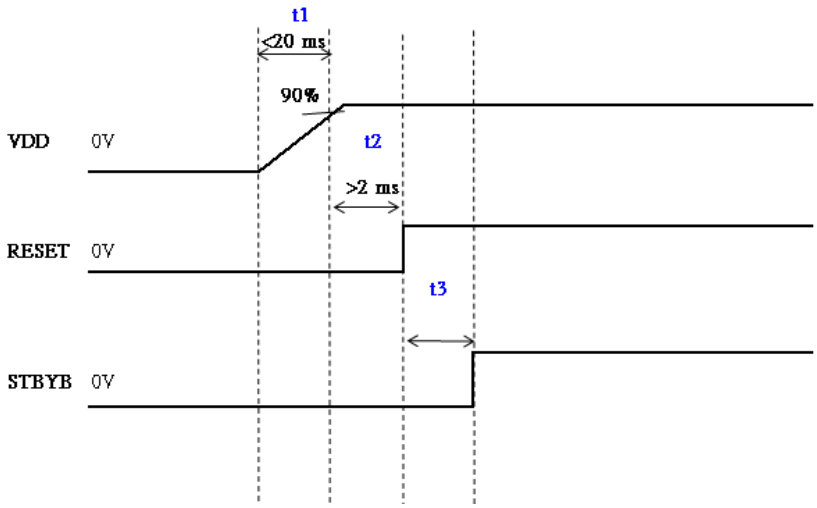
Refer to the figure as below:



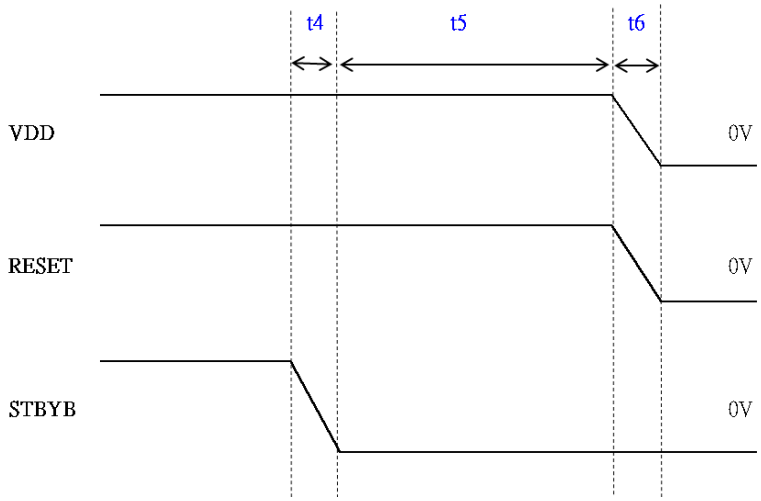
4.5 POWER ON/OFF TIMING SEQUENCE

The recommended power on sequence should be: VDD → RESET → STBYB. To power off, reverse this sequence, or turn off all signals and power simultaneously.

Power on：

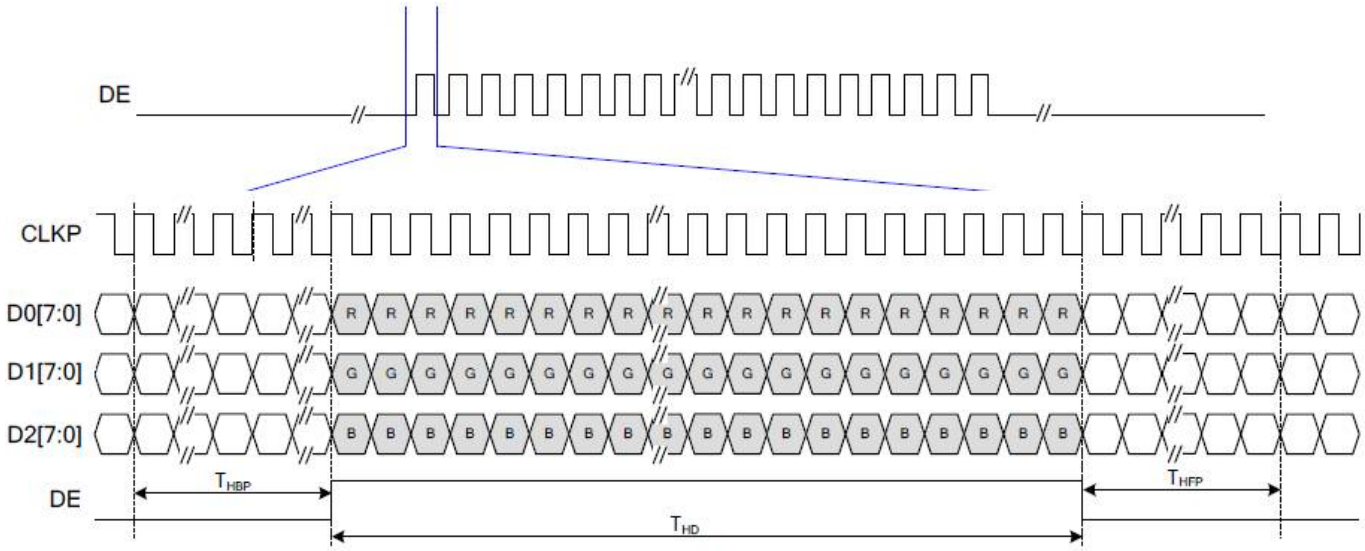


Power off：



Symbol	SPEC.			Unit
	Min.	Typ.	Max.	
t1	0	5	20	ms
t2	2	3	5	ms
t3	0	5	10	ms
t4	0	2	5	ms
t5	8	9	10	frame
t6	0	2	5	ms

4.6 Data Input Format for TTL



4.7 Input Timing

Only DE mode for 800x480

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	F_{CLK}	25.2	25.4	35.7	MHz
Horizontal display area	T_{HD}		800		CLK
HS period time	T_H	860	864	974	CLK
HS blanking	$T_{HFP} + T_{HBP}$	60	64	174	CLK
Vertical display area	T_{VD}		480		H
VS period time	T_V	488	490	611	H
VS blanking	$T_{VBP} + T_{VFP}$	8	10	131	H

4.8 DC Electrical Characteristics

TTL Interface DC Characteristic：

(VDD= 3.0V to 3.6V, GND= 0V, Ta= +25°C)

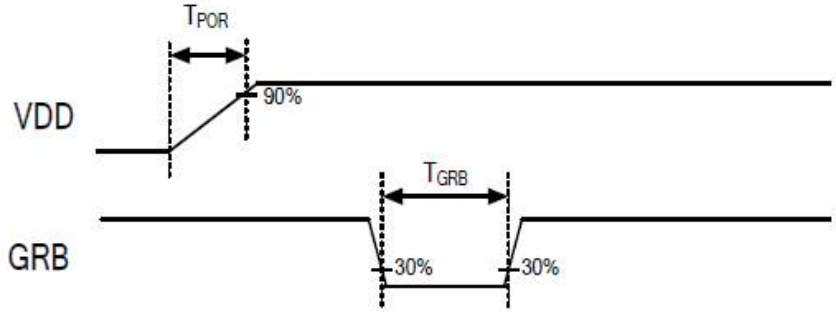
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
High Level Input Voltage	V_{IH}	0.7xVDD	-	VDD	V	
Low Level Input Voltage	V_{IL}	GND	-	0.3xVDD	V	
High Level Output Voltage	V_{OH}	VDD-0.4	-	VDD	V	VDD=3.3V @Ioh= 1mA
Low Level Output Voltage	V_{OL}	GND	-	GND+0.4	V	VDD=3.3V @Iol= -1mA
Pull-high/low Impedance	R_{PULL}	100	250	500	Kohm	VDD=3.3V, Ta =+25℃

4.9 AC Electrical Characteristics

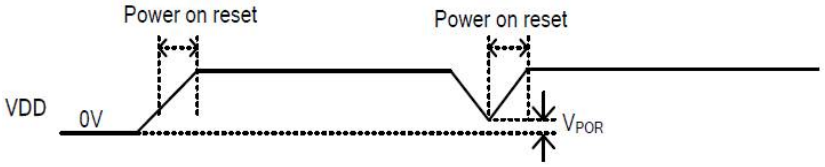
Basic Input AC Characteristic：

(VDD= 3.0V to 3.6V, GND= 0V, Ta= +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD power source slew time	T_{POR}	-	-	20	ms	From 0V to 90% VDD
GRB active pulse width	T_{GRB}	1	-	-	ms	VDD = 3.3V
Power on reset voltage	V_{POR}	0	-	100	mV	



Basic AC Timing Chart

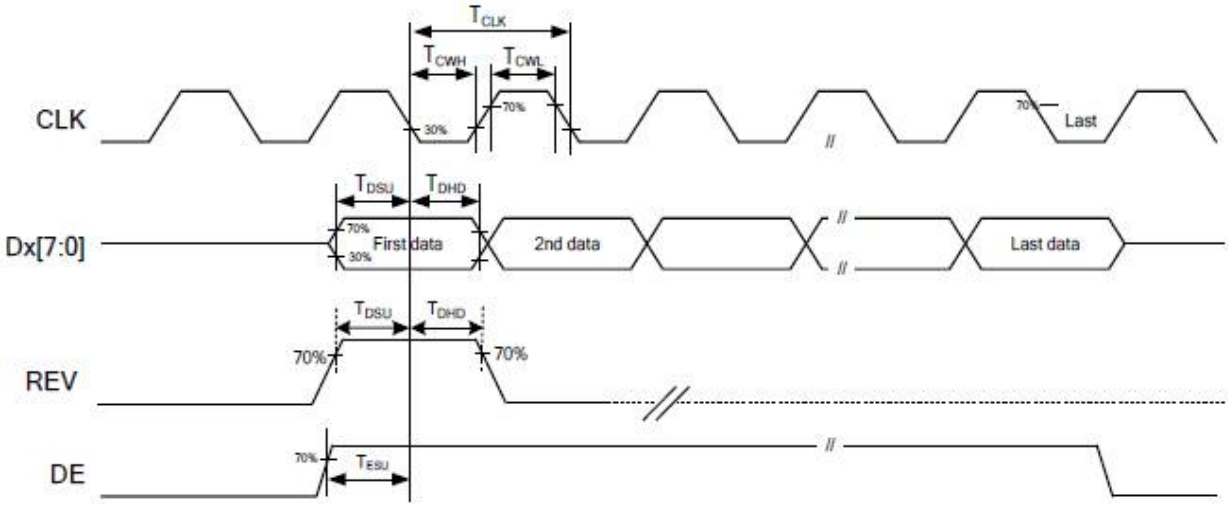


Power On Reset Chart

TTL-DE Interface AC Characteristic：

(VDD= 3.0V to 3.6V, GND= 0V, Ta= +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	F_{CLK}	5	-	55	MHz	$T_{CLK} = 1/F_{CLK}$
CLK pulse width	T_{CW}	30% (*)	-	70%	T_{CLK}	(*) Over than $0.5/(F_{CLK})_{max.}$
Data setup time	T_{DSU}	6	-	-	ns	
Data hold time	T_{DHD}	6	-	-	ns	
DE setup time	T_{ESU}	6	-	-	ns	



5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

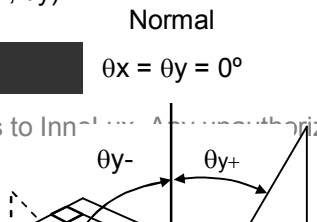
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25	°C
Ambient Humidity	Ha	50	%RH
Supply Voltage	VDDI		V
	VCI		V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L		mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Horizontal	x+	CR > 10	80	-	-	Deg.	(1), (4), (5)
		x-		80	-	-		
	Vertical	y+		80	-	-		
		y-		80	-	-		
Transmittance		T%	θ_x=0°, θ_Y =0°	3.9	4.5	-	%	(4), (5)
Contrast Ratio		CR		800	1000	-	-	(2), (4), (5)
Response Time		$T_{R+}T_F$		-	25	35	ms	(3), (5)
Color Coordinates	White	Wx		0.272	0.312	0.352	-	Panel under C light
		Wy		0.327	0.367	0.407		
	Red	Rx		0.621	0.661	0.701		
		Ry		0.287	0.327	0.367		
	Green	Gx		0.242	0.282	0.322		
		Gy		0.536	0.576	0.616		
	Blue	Bx		0.094	0.134	0.174		
		By		0.065	0.105	0.145		
NTSC					68	-	%	

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

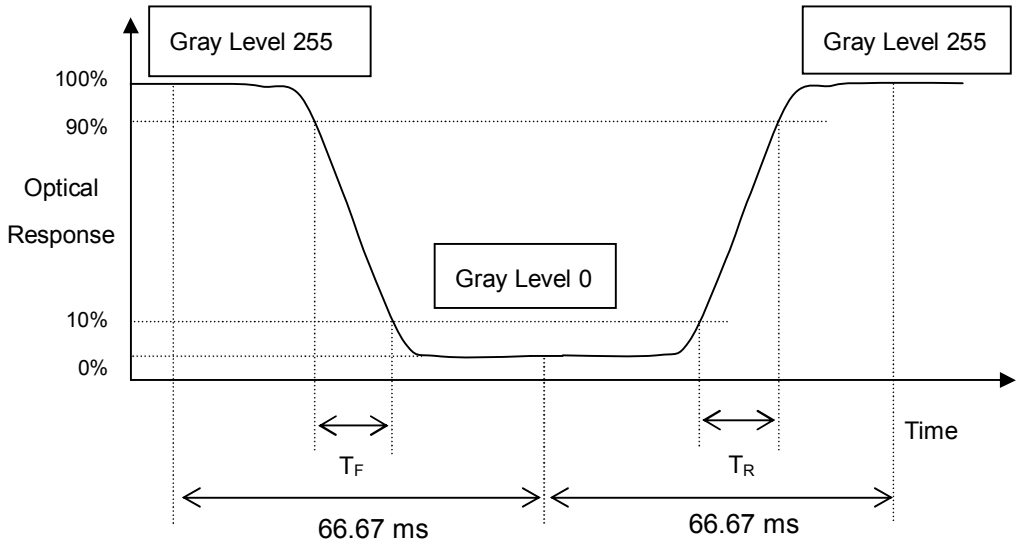
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

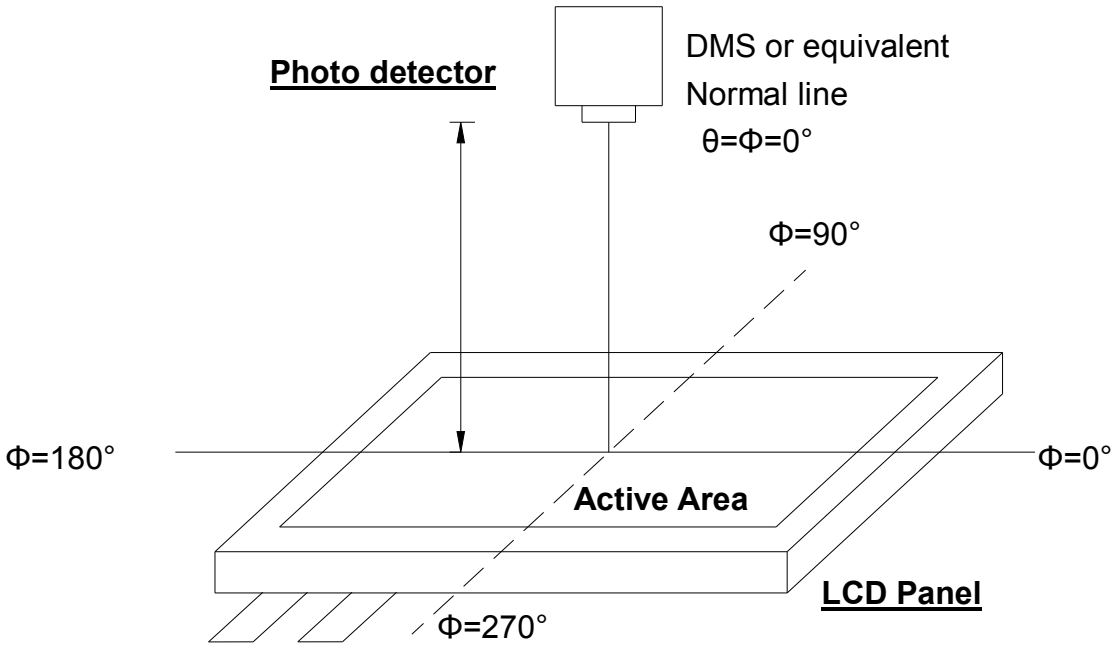
CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (5) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	Ta=90ºC, 500 hours	Note 1 Note 2 Note 3 Note 4
Low Temperature Storage Test	Ta=-40ºC, 500 hours	
High Temperature Operation Test	Tp=85ºC, 500 hours	
Low Temperature Operation Test	Ta=-30ºC, 500 hours	
High Temperature & High Humidity Operation Test	Ta=60ºC, RH 90%, 500hours	
Thermal Shock	[(-40℃ 30min)→(90℃ 30min)]/cycle , 100cycles	

Note 1: Ta = Ambient Temperature, Tp = Panel Surface Temperature.

Note 2: Criteria: Normal display image with no obvious non-uniformity and no line defect.

Note 3: Evaluation should be tested after storage at room temperature for more than two hour

Note 4: A certain level of Mura (non-uniformity) of dark / black image will happen several days after high temperature testing (H.T.T.). There is a slowly part recovery over a long time (several months). Such a long exposure time like in H.T.T. will normally not happen in a real application. Therefore the test H.T.T. was introduced to simulate cycles with normal conditions in-between but with the same total exposure time what show a significant reduced Mura.

The root cause is related to tension generated due to different amount of shrinking in the stack of layers in the polarizer sheet. The effect is more significant on larger displays like this size. An investigation into alternative polarizer material showed that there is no better alternative currently available.

7. PACKING

7.1 MODULE LABEL (Unit:mm)

7.2 PACKAGING METHOD

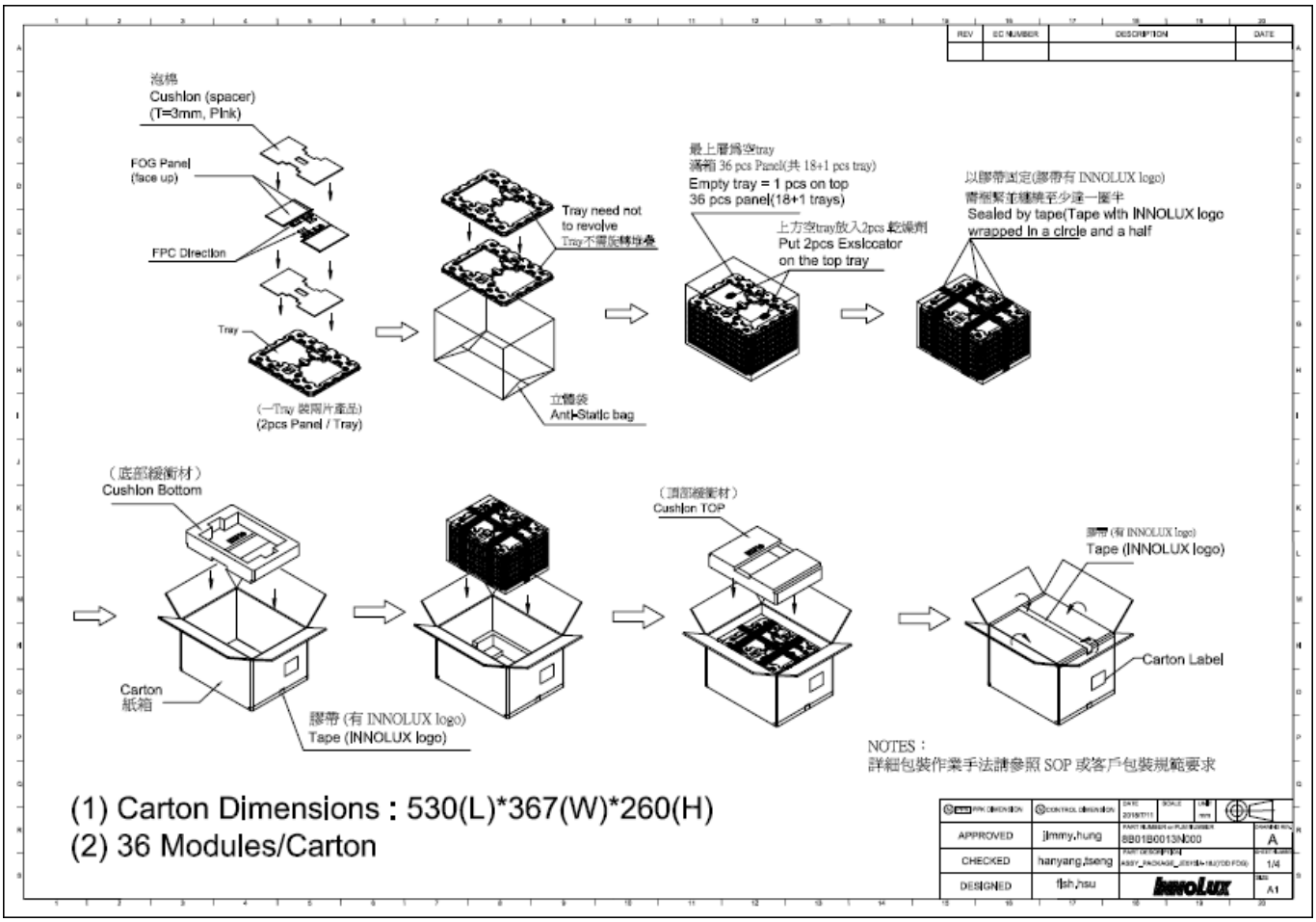


Figure. 7-1 Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

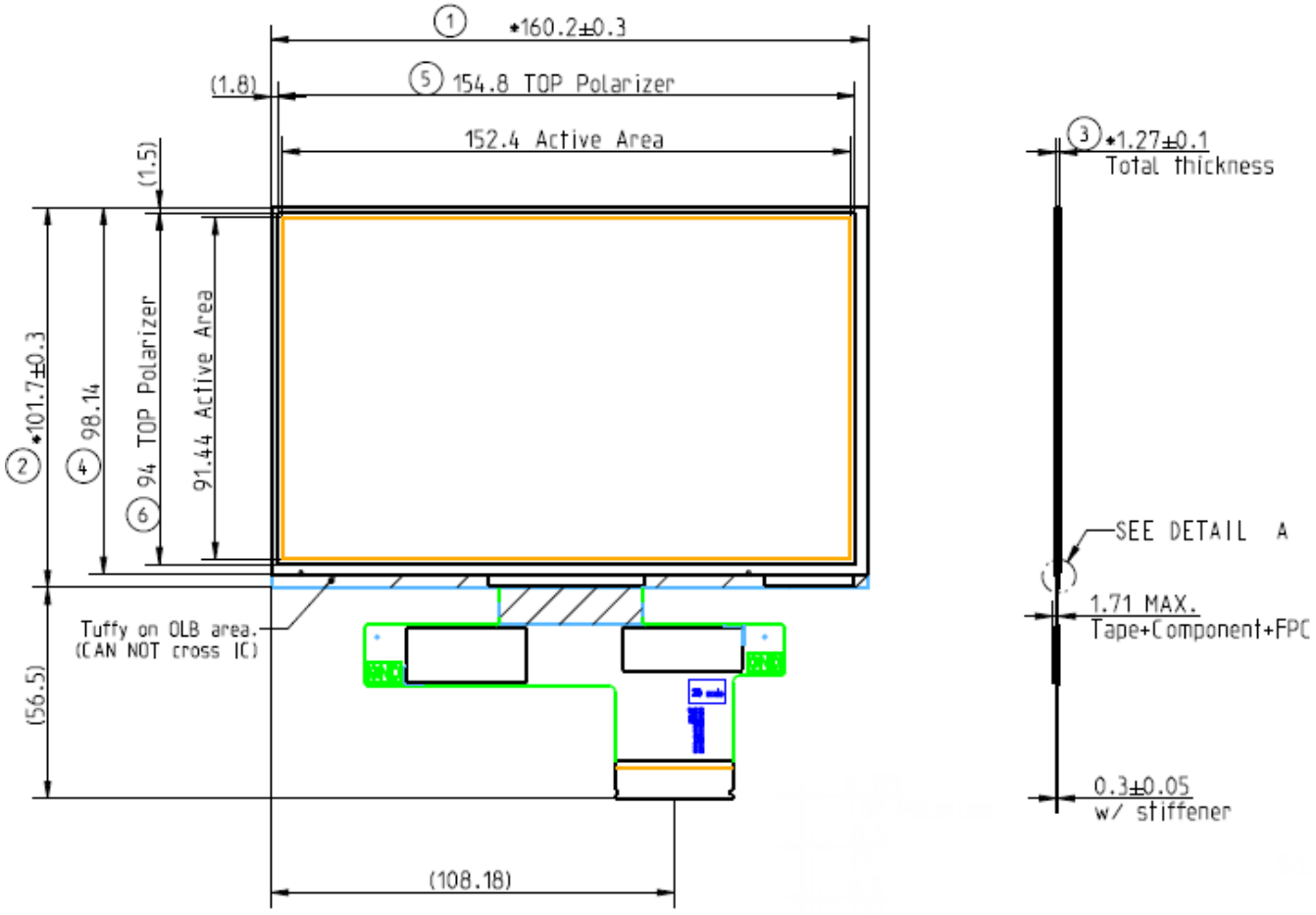
8.3 OPERATION PRECAUTIONS

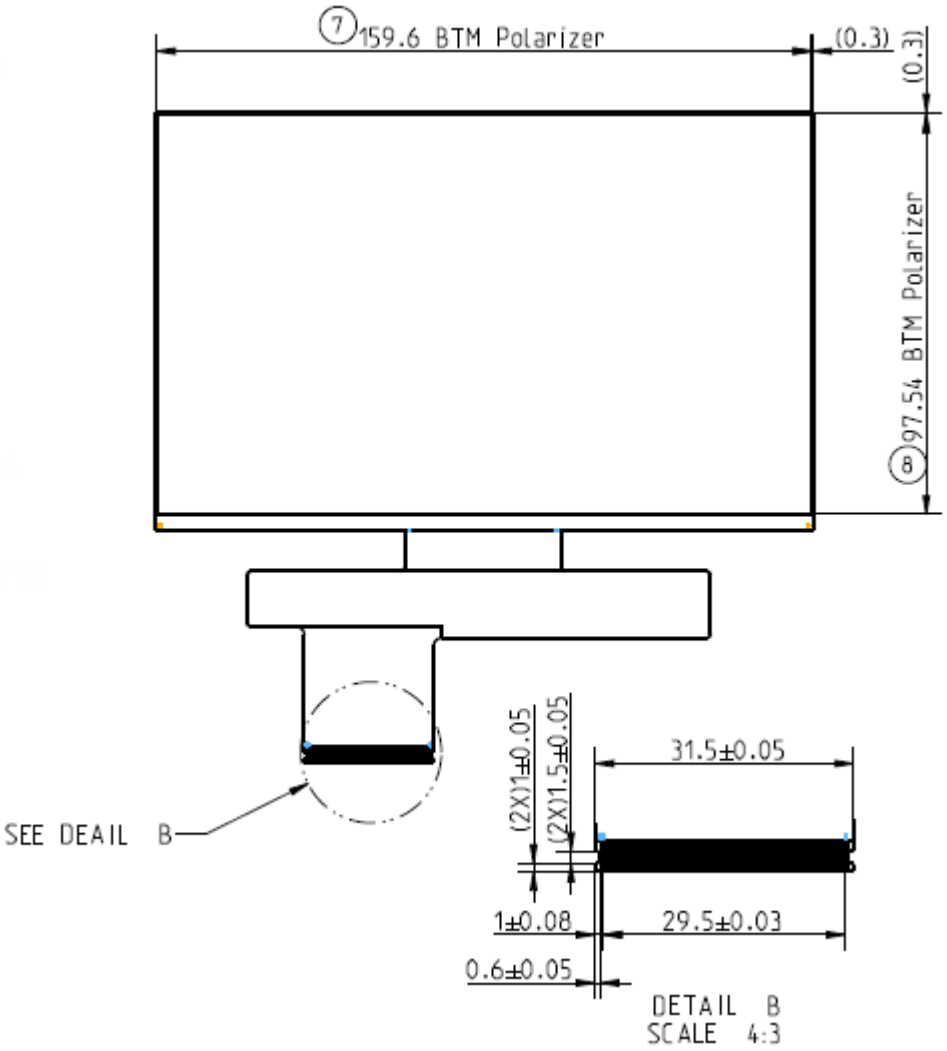
(1) Do not pull the I/F connector in or out while the module is operating.

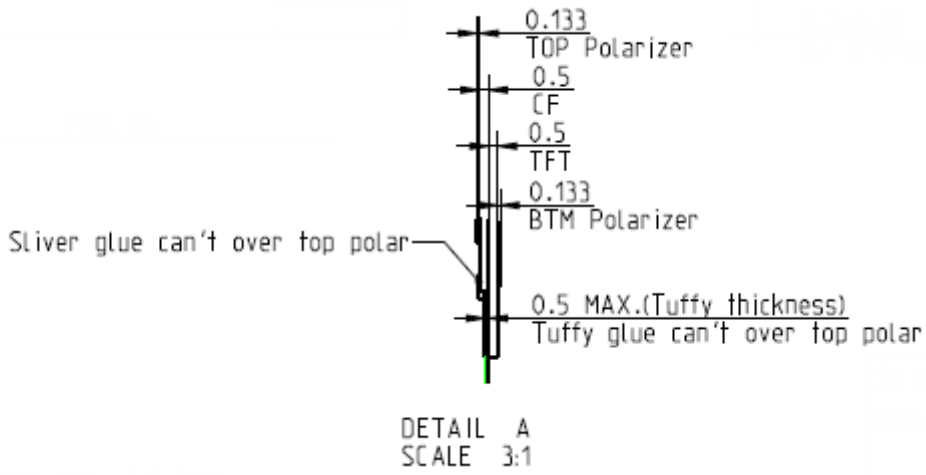
(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the backlight unit.

Appendix. OUTLINE DRAWING



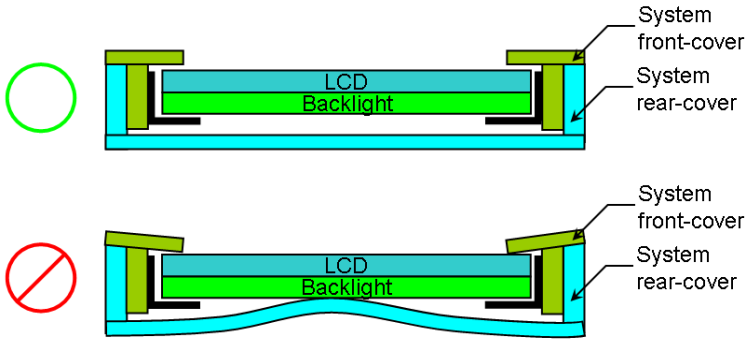
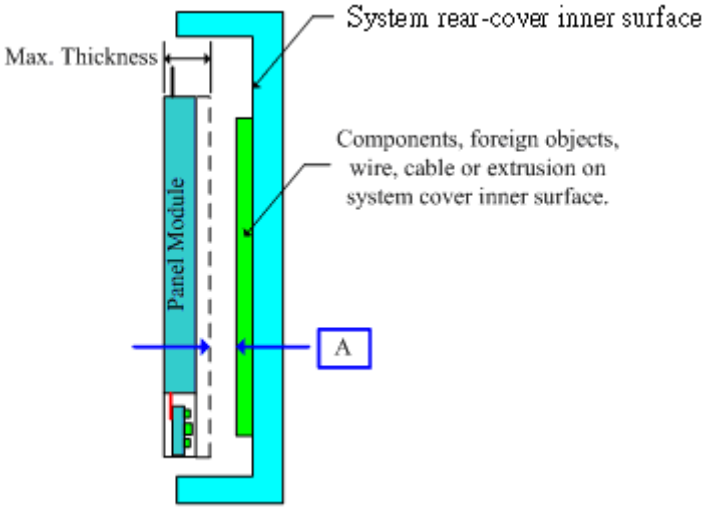


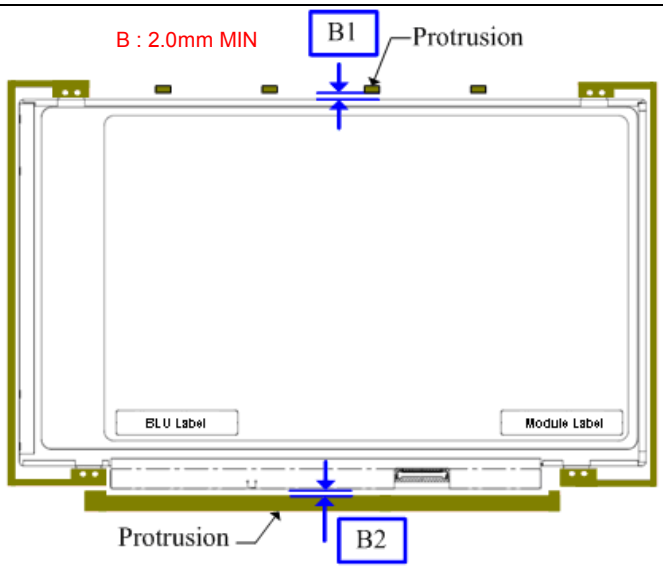


DETAIL A
SCALE 3:1

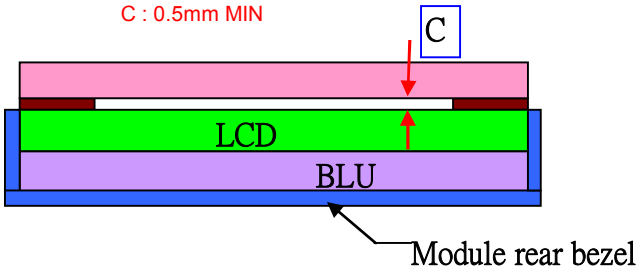
Notes:
-The dimensions without tolerance are +/-0.3mm.
-Dimensions marked with " *+balloon " is significant dimension.
Cpk>=1.33 , to be checked according " *+balloon " list : 1~3
-General dimensions numbered with " balloon " : 4-8
-Cannot guarantee for cosmetic defect outside of active area.
-All otherdimensins are for reference.

Appendix II. SYSTEM COVER DESIGN GUIDANCE

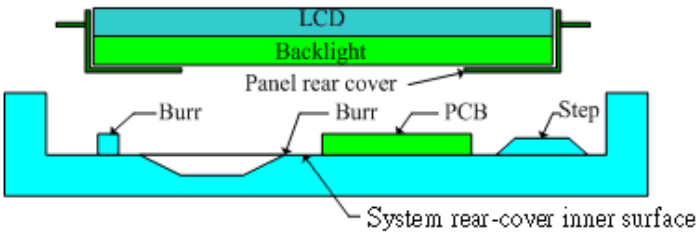
1.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
2.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
3	**Design gap B1 & B2 between panel & protrusions**



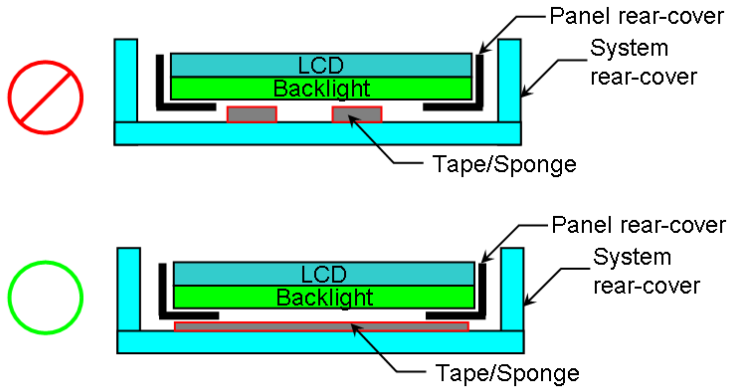
Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
4	**Design gap C between touch panel & panel surface.**



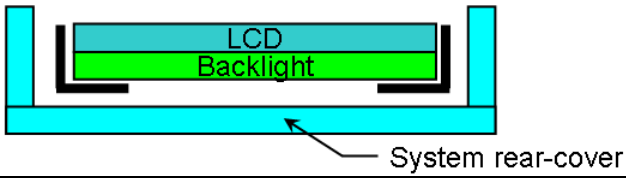
Definition	Air gap design between touch panel & panel surface is needed to prevent pooling, newton ring or glass broken. Compression ration of double side tape may cause pooling issue or newton ring. This phenomenon is obvious during pooling inspection procedure. To remain sufficient gap between touch panel and panel surface is recommended.
5	**System rear-cover inner surface examination**



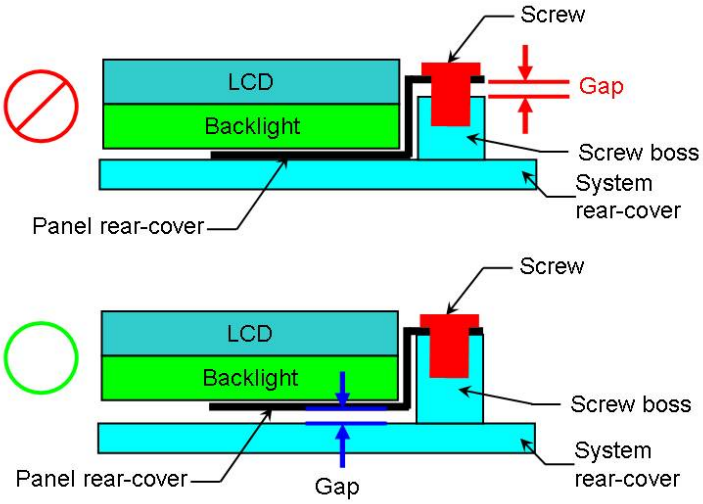
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
6	**Tape/sponge design on system inner surface**



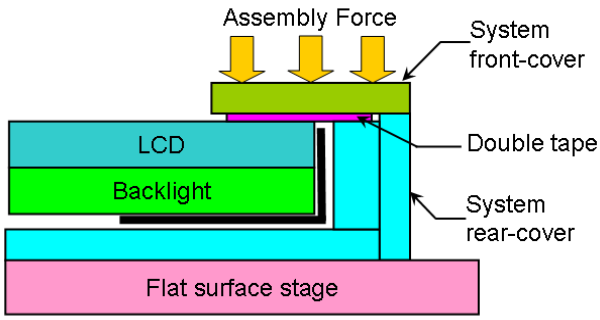
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7	**Material used for system rear-cover**



Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
8	**Screw boss height design**



Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
9	**Assembly SOP examination for touch panel with double side tape design**

	
Definition	To prevent panel crack during touch panel assembly process with double tape design, it is only allowed to give slight pressure with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.