TOROSON 炬 垄 森 科 技 厦门炬垄森科技有限公司

Xiamen Toroson Technology Co., Ltd

TFT-LCD Module

SPECIFICATION

Customer: _____

Model Name: VI104DI3C5

SPEC NO.: _____

Date: 2026.02.04

Version: V01

■ **Preliminary Specification**

□ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

SPEC NO.: VI104DI3C5 Date: 2026/01/19

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1. FEATURES

VI104DI3C5 is a transmissive type color active matrix liquid crystal module (LCM), which uses amorphous thin film transistor (TFT) as switching devices. This module has a 10.4 inches diagonally measured active display area with 800 x 600 resolution.

2. GENERAL SPECIFICATIONS

Item	Description	Unit
Display Size	10.4	inch
Display Type	Transmissive, a-Si	-
Active Area (HxV)	211.2 (H) x 158.4 (V)	mm
Number of Dots (HxV)	800 x RGB x 600	dot
Pixel Pitch(HxV)	0.264 x 0.264	mm
Color Arrangement	RGB Stripe	-
Color Numbers	16.7 M	-
Transmissive Mode	Normally black	-
Outline Dimension (HxVxT)	228.4 (H) x 175.4(V) x 5.9 (T)	mm
NTSC (CIE1931) (Under C light)	65 (Typ.)	%
Response Time	≤35	ms
Viewing Angle (Light On) (R/U/L/D)	80°/80°/80°/80°(R/U/L/D) (Min.)	
Surface Treatment	Front : AG Rear : Plain	
Contrast Ratio (Light On)	1000:1 (Typ.)	
Operation Temperature	-20~70	℃
Storage Temperature	-20~70	℃
Interface	LVDS	
Weight	350	g
Driver IC	S_IC：HX82103-A00DPD2000-P G_IC：HX8691-A01APD200-P	

3. PIN DESCRIPTION

FPC Connector is used for the module electronics interface. The recommended model is FH12A-40S-0.5SH manufactured by Hirose.

Pin No.	Symbol	I/O	Function	Remark
1	VCOM	P	Common Voltage	
2	VDD	P	Power Voltage for digital circuit	
3	VDD	P	Power Voltage for digital circuit	
4	NC	---	No connection	
5	RESET	I	Global reset pin	
6	STBYB	I	Standby mode, Normally pulled high STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z	
7	GND	P	Ground	
8	RXIN0-	I	- LVDS differential data input	
9	RXIN0+	I	+ LVDS differential data input	
10	GND	P	Ground	
11	RXIN1-	I	- LVDS differential data input	
12	RXIN1+	I	+ LVDS differential data input	
13	GND	P	Ground	
14	RXIN2-	I	- LVDS differential data input	
15	RXIN2+	I	+ LVDS differential data input	
16	GND	P	Ground	
17	RXCLKIN-	I	- LVDS differential clock input	
18	RXCLKIN+	I	+ LVDS differential clock input	
19	GND	P	Ground	
20	RXIN3-	I	- LVDS differential data input	
21	RXIN3+	I	+ LVDS differential data input	
22	GND	P	Ground	
23	NC	---	No connection(reserved for INX test)	Note1
24	NC	---	No connection(reserved for INX test)	Note1

25	GND	P	Ground	
26	NC	---	No connection	
27	NC	---	No connection	
28	SELB	I	6bit/8bit mode select (not floating) SELB=0: 6bit; SELB=1: 8bit (default)	
29	AVDD	P	Power for Analog Circuit	
30	GND	P	Ground	
31	NC	---	No connection	
32	NC	---	No connection	
33	LR	I	Horizontal inversion	Note2
34	UD	I	Vertical inversion	Note2
35	VGL	P	Gate OFF Voltage	
36	LVDS_FMT	I	LVDS format select LVDS_FMT=0：JEIDA LVDS_FMT=1 or NC：VESA(default)	
37	NC	---	No connection	
38	VGH	P	Gate ON Voltage	
39	NC	---	No connection	
40	NC	---	No connection	

I: input, O: output, P: Power

Note 1: Pin 23 & 24 are used as I2C interface for INX test, keep these pin floating.

Note 2:

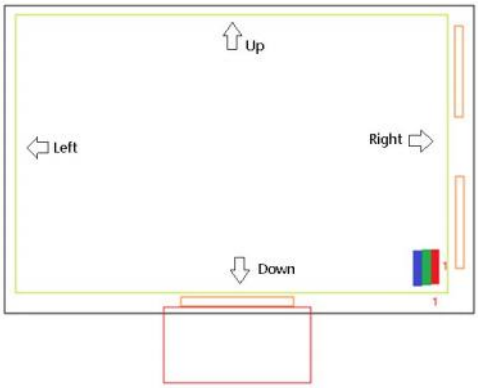
LR & UD control driver IC scan direction, refer to blow picture:

LR= 1: from LEFT to RIGHT

LR= 0: from RIGHT to LEFT

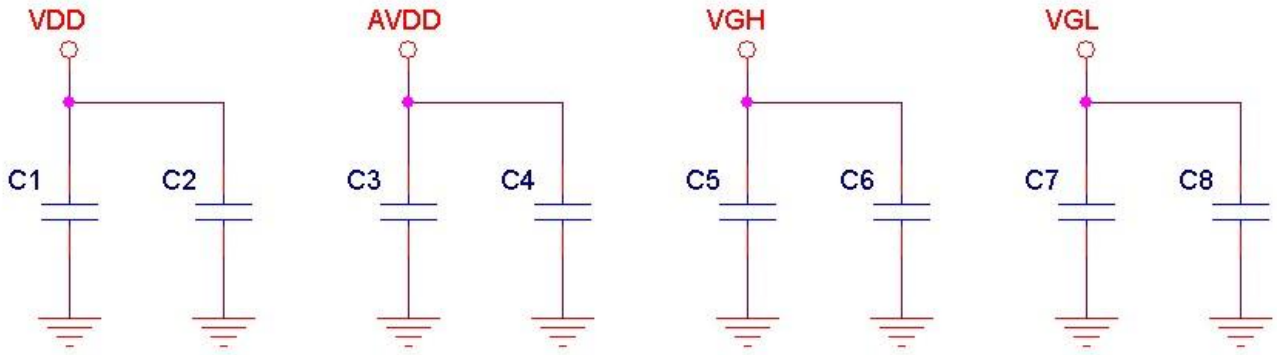
UD= 1: from UP to DOWN

UD= 0: from DOWN to UP

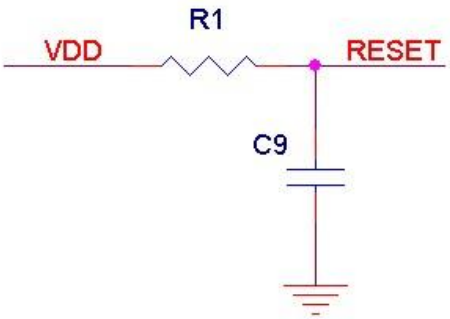


3.1 Advice circuit for customer system

3.1.1 Power PIN: AVDD/VDD/VGH/VGL



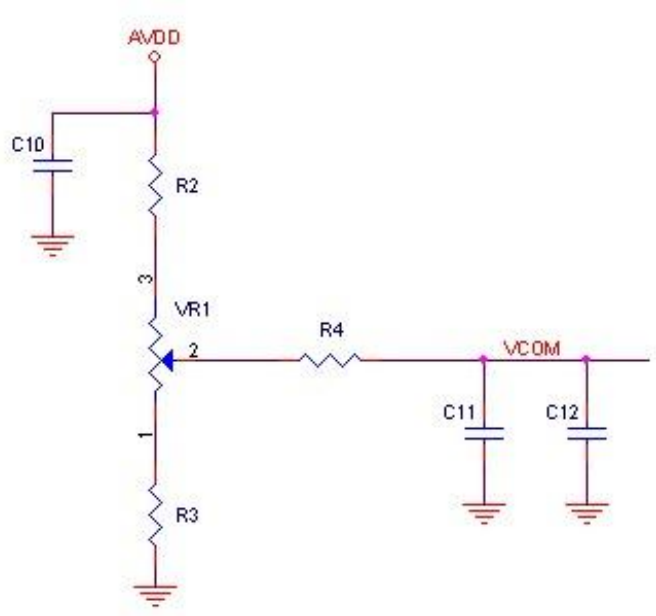
3.1.2 Control PIN: RESET or connect to control IC GPIO.



3.1.3 VCOM

Typical VCOM is only a reference value, it must be optimized according to each LCM. Be sure to use VR;

Or VCOM is output by power IC with auto just programmer VCOM function.



3.2 Suggestion BOM

Location	Description
C1,C11	10uF,X5R,10V
C2,C12	100nF,X5R,10V
C3,C7	10uF,X5R,25V
C4,C8	100nF,X5R,25V
C5	10uF,X5R,50V
C6	100nF,X5R,50V
C9	1uF,X5R,10V
C10	1uF,X5R,25V
R1	10Kohm,1%
R2	20Kohm,1%
R3	10Kohm,1%
R4	0ohm,1%
VR1	10Kohm,1%

4. ABSOLUTE MAXIMUM RATING

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	3.6	V	
	AVDD	-0.3	15	V	
	VGH	-0.3	30	V	
	VGL	-15	0.3	V	

Note:

(1) All of the voltages listed above are with respective to GND= 0V

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

Backlight Driving Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Voltage for LED backlight	V_L	16.2	17.4	20.4	V	Note 1
Current for LED backlight	I_L	220	240	260	mA	
LED life time	-	20,000	50000	-	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L =240mA. The LED lifetime could be decreased if operating I_L is lager than 240mA.

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5. DC CHARACTERISTICS

5.1 Parameter

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Power supply voltage	VDD	3.0	3.3	3.6	V	
	AVDD	12.8	13.0	13.2	V	
	VGH	26.5	27.0	27.5	V	
	VGL	-10.5	-10.0	-9.5	V	
Input signal voltage	VCOM	4.9	5.5	6.0	V	
Ripple Voltage	VDD VRP	-	50	100	mV	
	VRP	-	50	200	mV	Note 1
Logic high level input voltage	VIH	0.8xVDD	-	VDD	V	Note 2
Logic low level input voltage	VIL	0	-	0.2xVDD	V	

(Ta = 25 ± 2℃)

Note 1: Inculding Power: AVDD、VGH、VGL & VCOM.

Note 2: Including signal: UD、LR、RESET、STBYB、SELB.

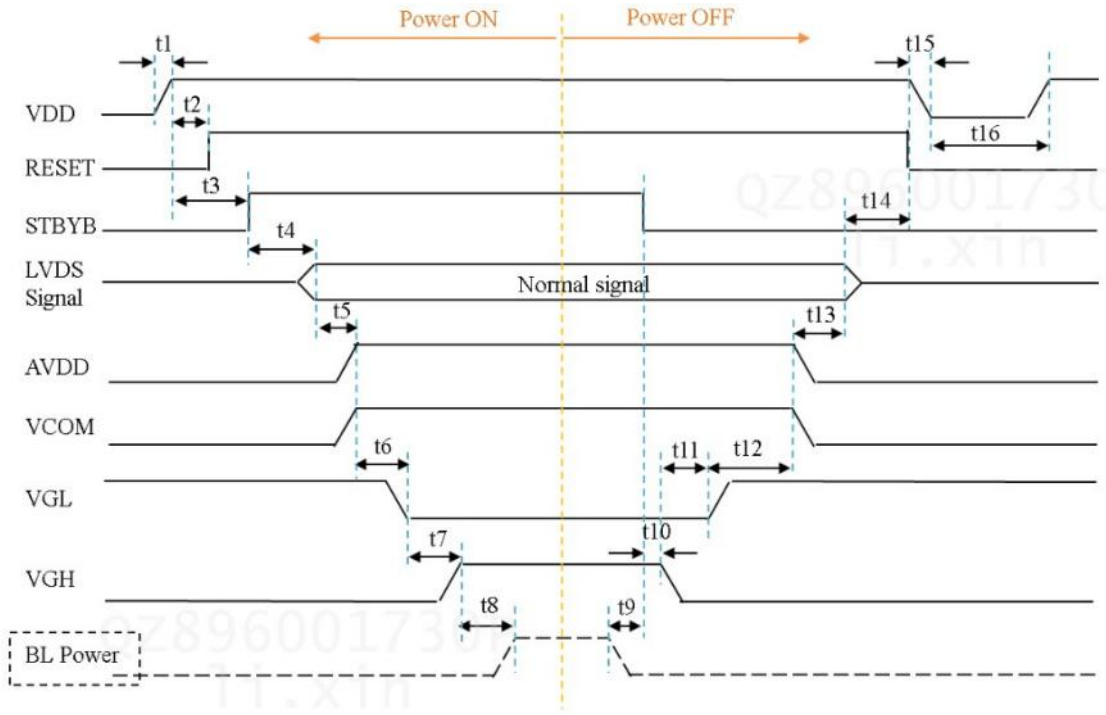
5.2 Current Consumption

Item	Symbol	Value			Units	Remark
		Min	Typ	Max		
Current for Driver	IVDD	15	25	35	mA	Note 1
	IAVDD	8	45	65	mA	Note 1
	IVGH	0.1	0.6	2	mA	Note 1
	IVGL	0.1	0.6	2	mA	Note 1

Note 1：The specified power supply current is under the conditions at VDD=3.3V，AVDD=13V，VGH=27V，VGL=-10V, Ta = 25 ± 2 ºC, DC Current and fv = 60 Hz, whereas a power dissipation check white pattern.

5.3 Power Sequence

Power on /off



Note: BL power & BL unit are designed by customer system.

Power on off timing

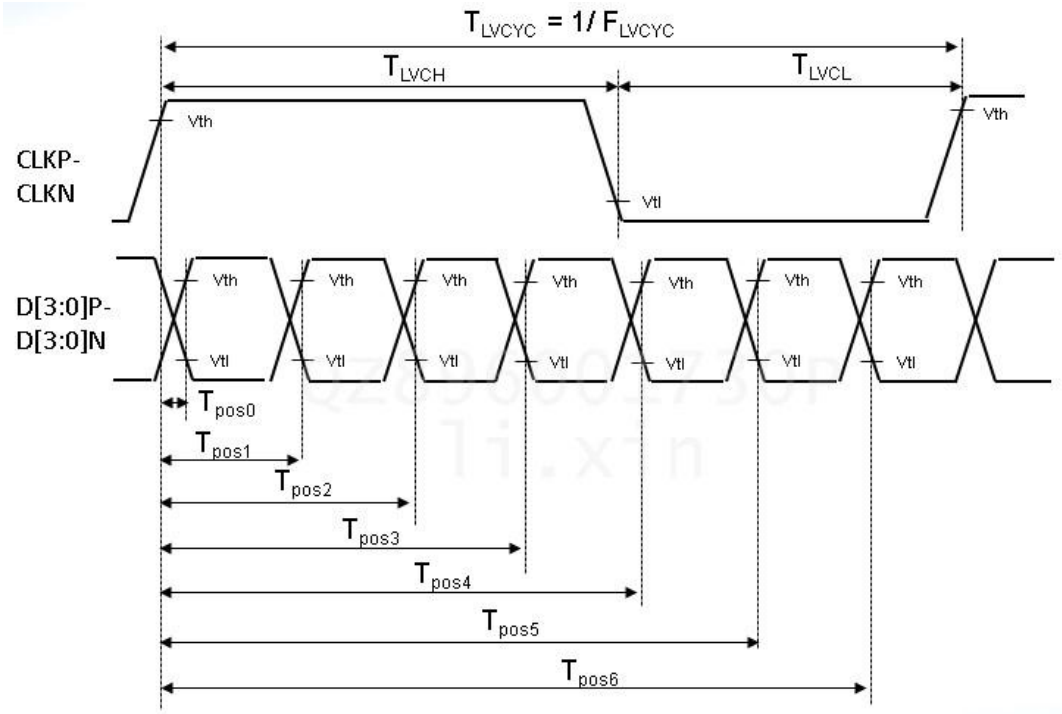
Symbol	SPEC			Unit
	Min.	Typ.	Max.	
t1	0.5	10	20	ms
t2	1	10	12	ms
t3	1	5	50	ms
t4	50	-	-	ms
t5	5	-	-	ms
t6	20	-	-	ms
t7	20	-	-	ms
t8	150	-	-	ms
t9	150	-	-	ms
t10	80	-	-	ms
t11	20	-	-	ms
t12	20	-	-	ms
t13	20	-	-	ms
t14	20	-	-	ms
t15	0.5	10	20	ms
t16	500	-	-	ms

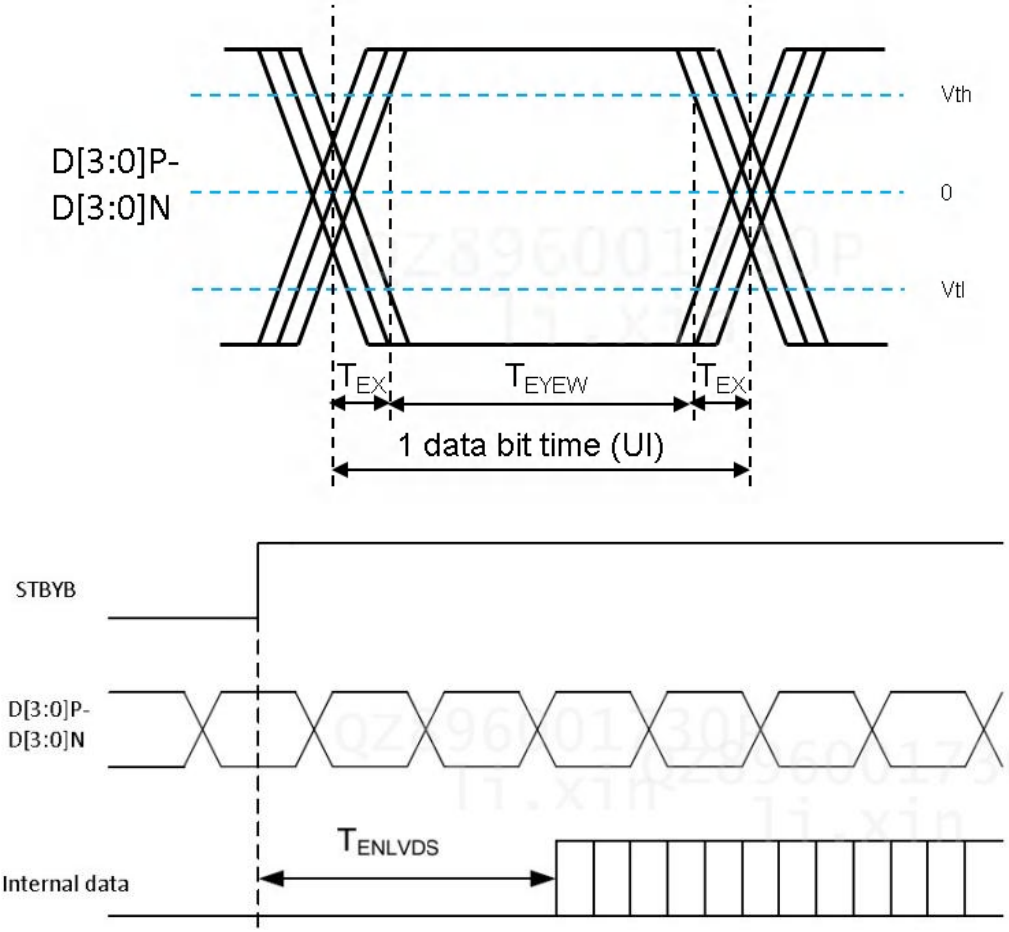
6. LVDS TIMING CHARACTERISTICS

6.1 AC Electrical Characteristics of LVDS

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	F_{LVCYC}	32.27	-	50.4	MHz
Clock period	T_{LVCYC}	19.84	-	-	ns
1 data bit time	UI	-	$1/7T_{LVCYC}$	-	ns
Clock high time	T_{LVCH}	-	4	-	UI
Clock low time	T_{LVCL}	-	3	-	UI
Position 0	T_{POS0}	-0.2	0	0.2	UI
Position 1	T_{POS1}	0.8	1	1.2	UI
Position 2	T_{POS2}	1.8	2	2.2	UI
Position 3	T_{POS3}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 5	T_{POS5}	4.8	5	5.2	UI
Position 6	T_{POS6}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.5	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake-up time	T_{ENLVDS}	-	-	150	us

6.2 Input LVDS Clock and Data Timing Diagram





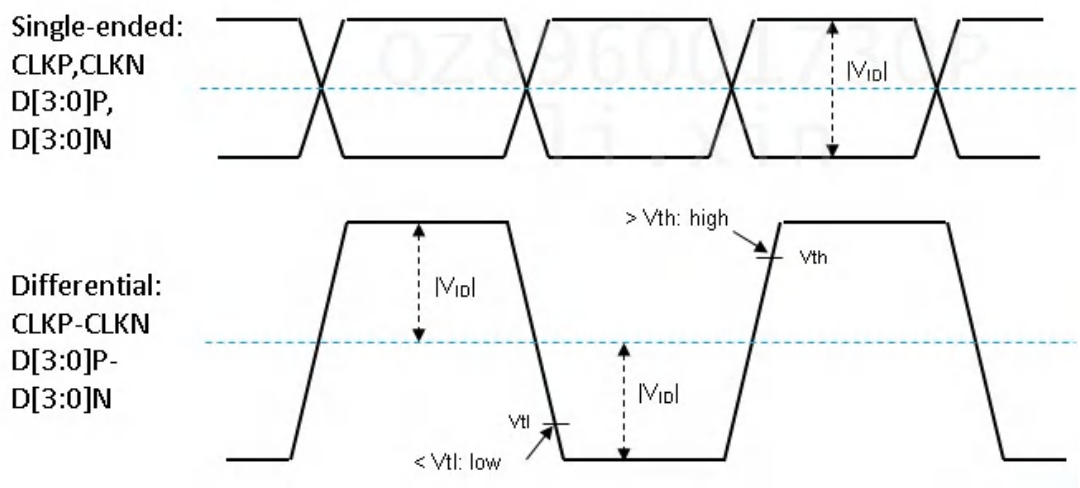
6.3 LVDS with SSC

The LVDS receiver can support spread spectrum clock (SSC). Limitation is listed as below.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max	
Modulation frequency	SSC_{MF}	LVDS clock frequency center at 85MHz	-	-	200	KHz
		LVDS clock frequency center at 60MHz	-	-	150	KHz
		LVDS clock frequency center at 40MHz	-	-	100	KHz
		LVDS clock frequency center at 20MHz	-	-	50	KHz
		LVDS clock frequency center at 15MHz	-	-	25	KHz
Modulation rate	SSC_{MR}	LVDS clock frequency + SSCMR in the range of 15MHz~85MHz	-	-	±3	%

6.4 Electrical Characteristics of LVDS

Parameter	Symbol	Min	Typ	Max	Units	Condition
Differential input high threshold voltage	V_{TH}	+0.1	-	-	V	V_{CM}=1.2V
Differential input low threshold voltage	V_{TL}	-	-	-0.1	V	
LVDS Input voltage	V_{INLV}	0.7	-	1.7	V	
Differential input common mode voltage	V_{CM}	0.45	1.2	1.7-|VID|/2	V	
Differential input voltage	|VID|	0.2	-	0.6	V	
Differential input leakage current	I_{Ivleak}	-10	0	+10	uA	
LVDS Differential impendence	Zdiff	90	100	110	ohm	D[3:0]P/N, CLKP/N

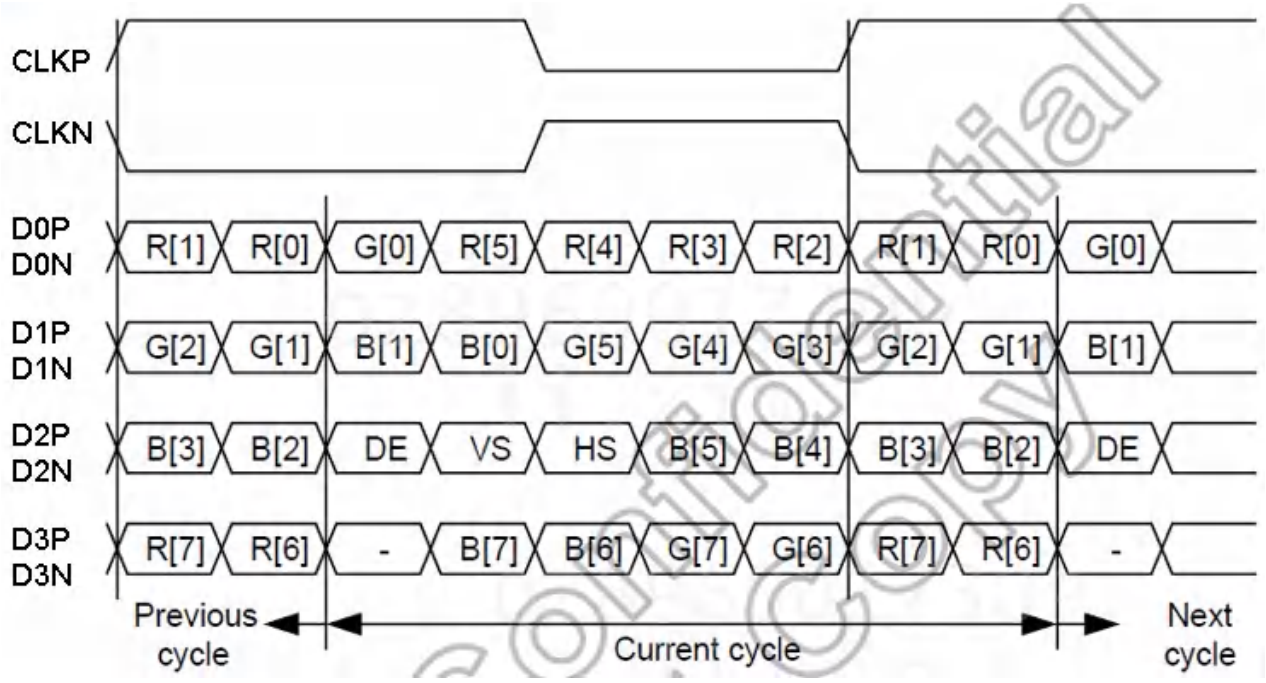


6.5 Timing of LVDS

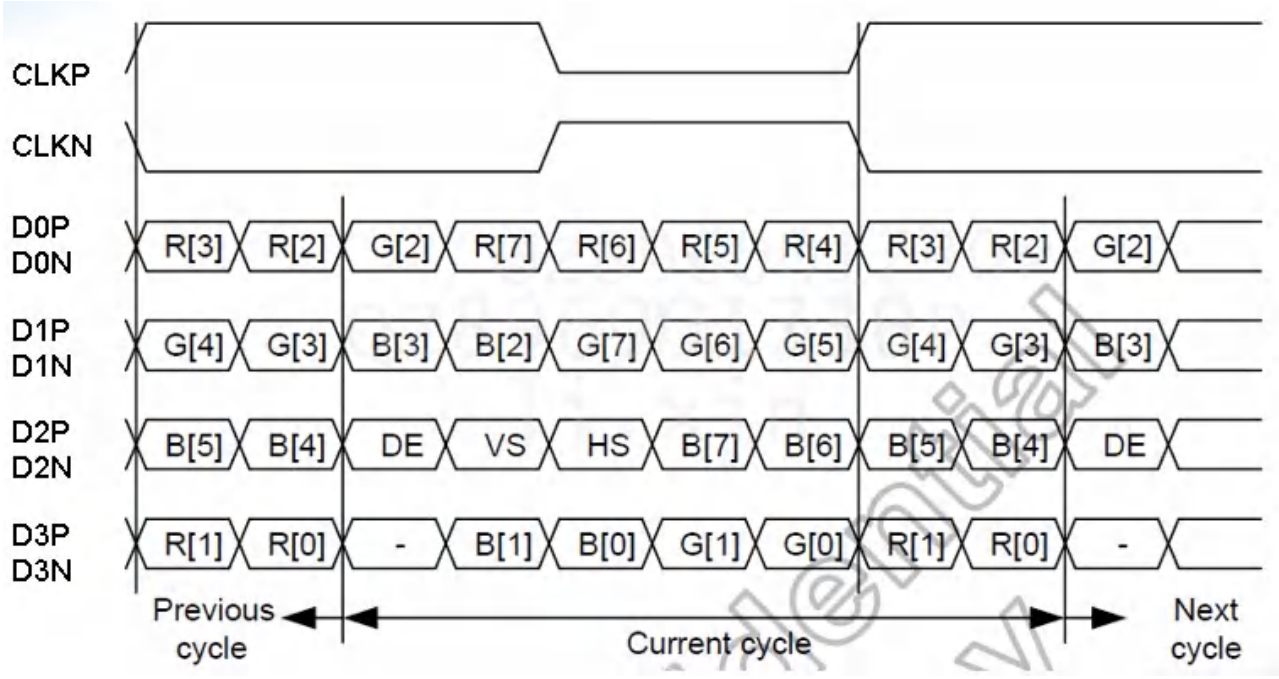
Parallel	Symbol	Vaule			Unit
		Min	Typ	Max	
DCLK Freqency Frame rate=60Hz	fclk	32.27	40.23	50.4	MHz
Horizontal display area	thd		800		DCLK
HSYNC period time	thpw	862	1056	1200	DCLK
HSYNC blanking	thb+thfp	62	256	400	DCLK
Vertical display area	tvd		600		H
VSYNC period time	tvpw	624	635	700	H
VSYNC blanking	tvb+tvfp	24	35	100	H

6.6 Data Input Format

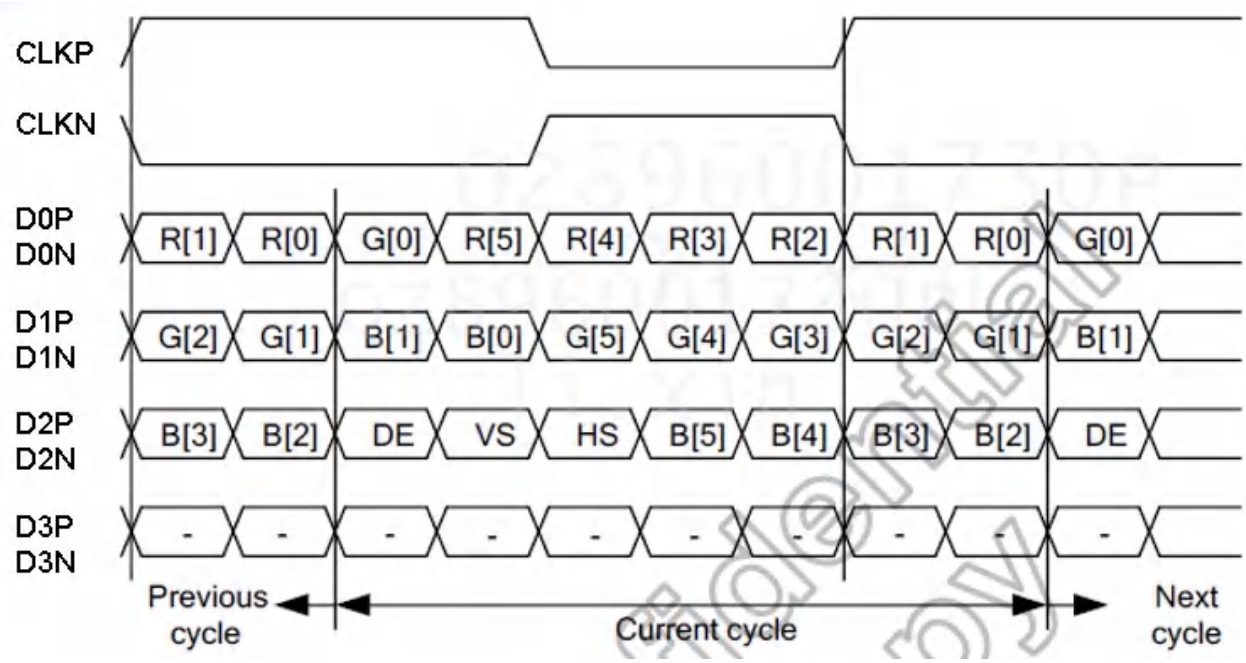
8bit LVDS input VESA format



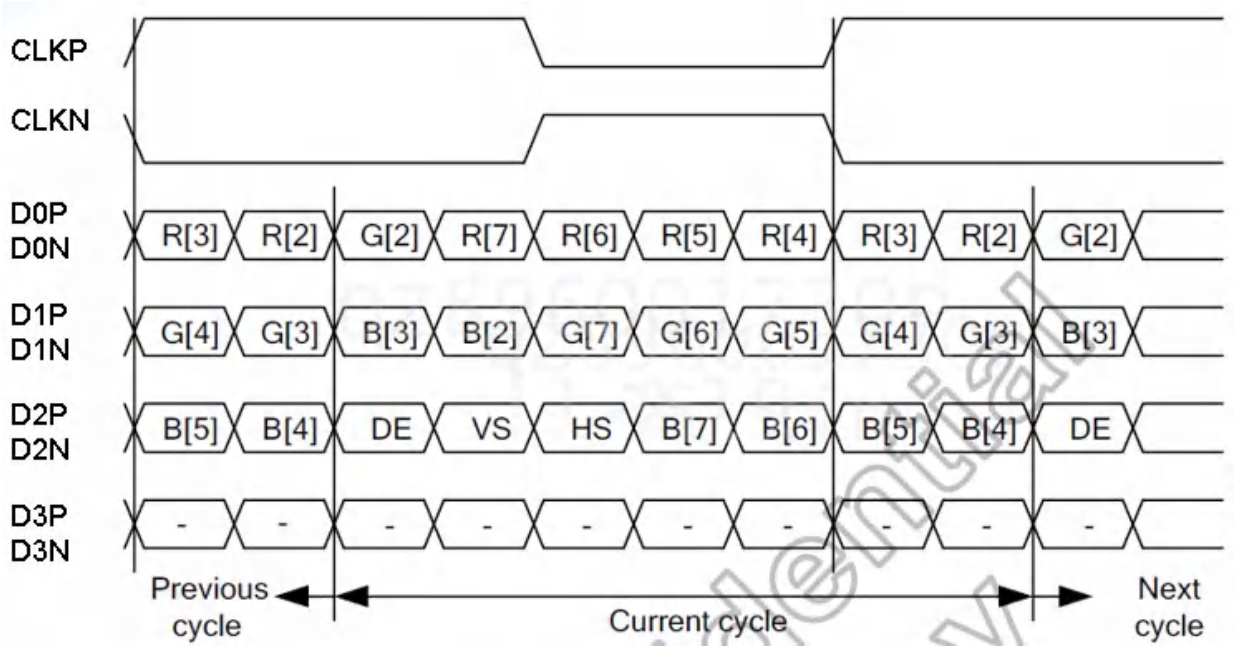
8bit LVDS input JEIDA format



6bit LVDS input VESA format



6bit LVDS input JEIDA format



7. OPTICAL CHARACTERISTICS

7.1 Optical Specification

Ta=25℃

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angles	θ 11(R)		CR ≥ 10	80	88	-	Degree	Note 7-1
	θ 12(L)			80	88	-		
	θ 21(U)			80	88	-		
	θ 22(D)			80	88	-		
Response Time	Tr+Tf		θ =0°	-	25	35	ms	Note 7-2
Luminance	L			250	300	-	cd/m^2	Note 7-3
Luminance uniformity	LU			70	75	-	%	Note 7-6
Contrast Ratio	CR			700	1000	-	-	Note 7-4
Chromaticity	White	x		0.285	0.335	0.385	-	*C Light Source* Note 7-5
		y		0.324	0.374	0.424		
	Red	x		0.605	0.655	0.705		
		y		0.285	0.335	0.385		
	Green	x		0.233	0.283	0.333		
		y		0.525	0.575	0.625		
	Blue	x		0.086	0.136	0.186		
		y		0.050	0.100	0.150		
NTSC	-			-	65	-	%	

7.2 Basic measure condition

(1) Driving voltage:

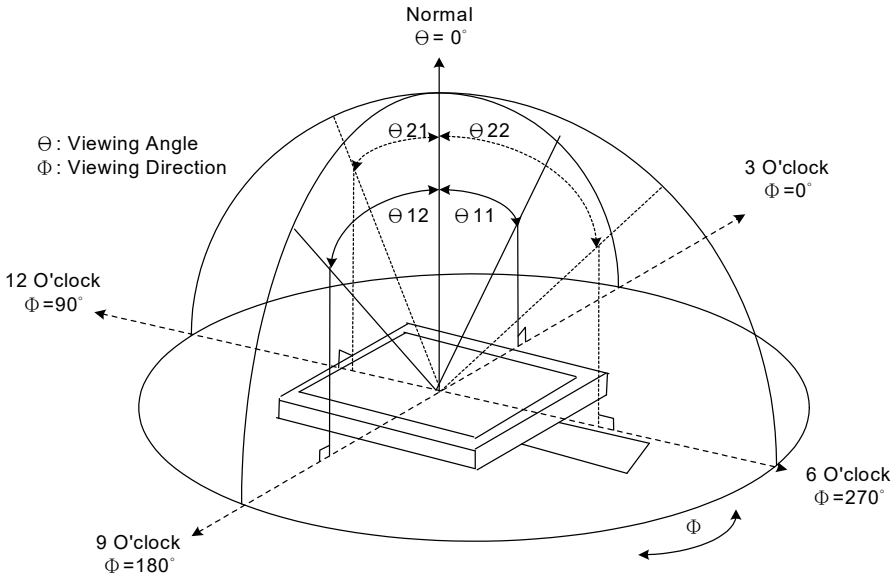
Based on item 5. DC CHARACTERISTICS and 6. LVDS TIMING CHARACTERISTICS

(2) Ambient temperature: Ta=25℃

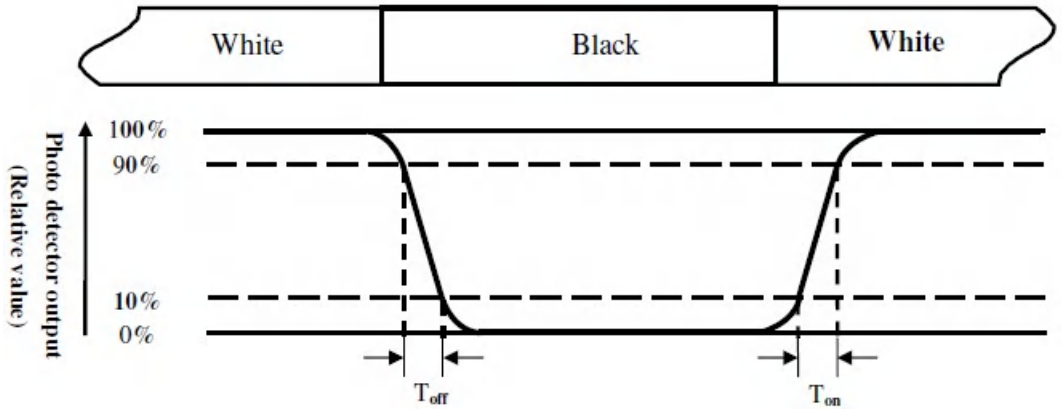
(3) Testing point: Measure in the display center point and the test angle θ =0°

(4) Testing facility: Environmental illumination: ≤ 10 Lux

Note 7-1: Viewing angle diagrams



Note 7-2: Response time



Note 7-3: Luminance

The brightness is measured at the center point of the module. .

Note 7-4: Contrast ratio

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = White / Black

Note 7-5 Chromaticity

The chromaticity is measured in CIE 1931 at the center point on C Light Source.

Note 7-6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

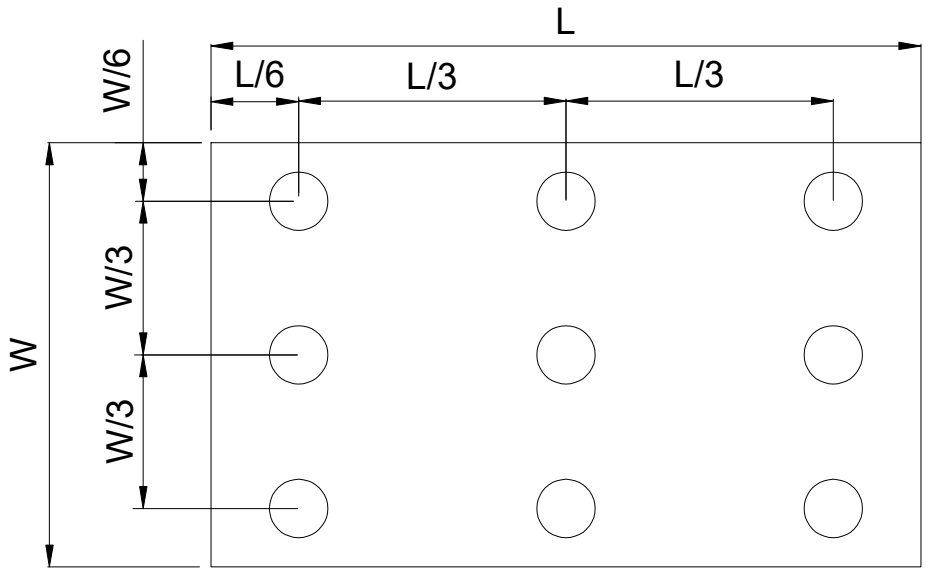


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.

8. QUALITY ASSURANCE

No.	Test Items	Test Condition	Note
1	High Temperature Storage	70℃, 240hrs	Note 1, 2
2	Low Temperature Storage	-20℃, 240hrs	Note 1, 2
3	High Temperature Operation	70℃, 240hrs	Note 1, 2
4	Low Temperature Operation	-20℃, 240hrs	Note 1, 2
5	High Temperature and High Humidity Storage	60℃, 90%RH, 240hrs	Note 1, 2
6	Thermal Shock	-20℃/0.5h ~ +70℃/0.5h for a total 100 cycles	Note 1, 2

Note 1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

Note 2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

9. HANDING CAUTIONS

9.1 ESD (Electrical Static Discharge) strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

(1) In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.

(2) The machine and working table for the panel should have ESD protection strategy.

(3) In handling the panel, ionized airflow decreases the charge in the environment is necessary.

(4) In the process of assemble module, shield case should connect to the ground.

9.2 Environment

(1) Working environment of the panel should be in the clean room.

(2) Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

9.3 Storage Precautions

(1) When storing for a long time, the following precautions are necessary.

(a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+-10%RH.

(b) The polarizer surface should not come in contact with any other object.

(c) It is recommended that they be stored in the container in which they were shipped.

(d) Storage condition is guaranteed under packing conditions.

(e)The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition

(2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(4) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

(5) Storage must be in a fully packaged state (PET bag) and do not expose the sample (module)

9.4 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature

and high humidity environment is prohibited.

(5) In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

(6) Unpacking (Hard Box) in order to prevent open cells broken:

[6.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[6.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[6.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[6.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.

[6.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[6.3.3] Do not press the surface of an open cell in a hard box.

[6.3.4] Do not pull X-board when an open cell placed in a hard box.

(7) Handling – In order to prevent open cells, COFs , and components damaged:

[7.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[7.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[7.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[7.4] Handle open cells one by one.

[7.5] In order to prevent driver IC from being injured by ESD, it is not recommended that the following positions be directly touched by hands.

(8) Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

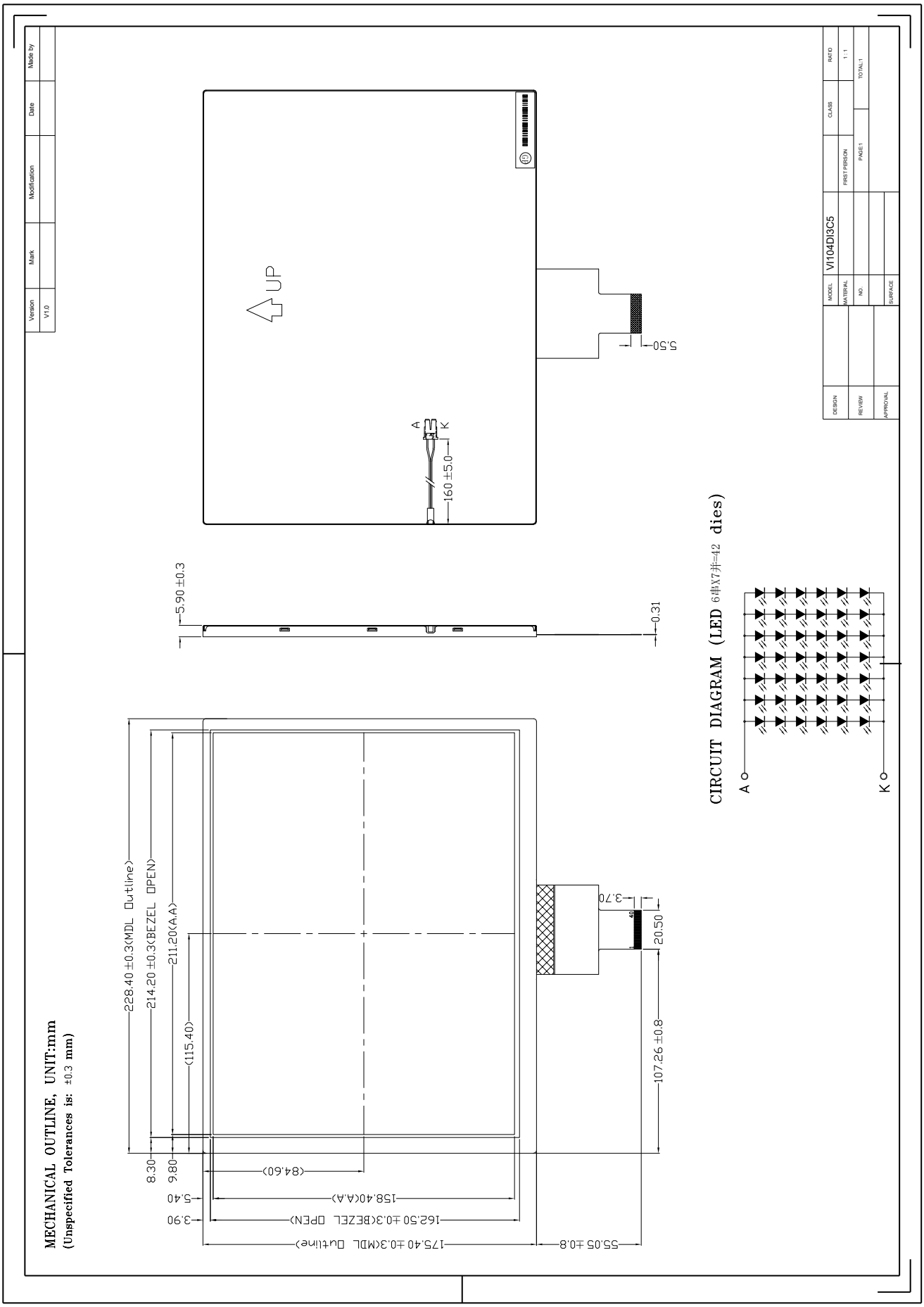
(9) Cleaning

[9.1] Do not wipe the polarizer with dry cloth. It might cause scratch.

[9.2] Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.

SPEC NO.: VI104DI3C5 Date: 2026/02/04

10. MECHANICAL DRAWING



11. PACKAGING DRAWING

TBD

11.2 Model Label

TBD