

TFT LCD Module SPECIFICATION

Customer: _____
Model Name: VI121VIC00
SPEC NO.: _____
Date: 2023.09.12
Version: V03

- Preliminary Specification
 Final Specification

For Customer's Acceptance

| Approved by | Comment |
|-------------|---------|
| | |

| Approved by | Reviewed by | Prepared by |
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Record of Revision

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| Version | Revise Date | Page | Content |
|---------|-------------|---------------|--|
| V02 | 2023.03.23 | 5 | Pin assignment modified for SEL68 |
| | | 15 | Modified the description of LVDS data input format of SEL 68 setting |
| | | 25 | modify back view |
| | | 26 | Add package information |
| V03 | 2023.04.26 | 4/9/ 17/20 | Update NTSC value、 Storage & Operation Temperature 、 NTSC、 Life time |
| | | 21 | Updated the backlight FPC position |

1. FEATURES

VI121VIC00 is a transmissive type color active matrix liquid crystal display Module(LCM), which uses amorphous thin film transistor (TFT) as switching devices. This panel has a 12.1 inches diagonally measured active display area with resolution 1024 x 768. This product is composed of a TFT LCD panel, polarizers, driver ICs, FPC and PCBA.

Note: Air-Bonding is recommended

2. GENERAL SPECIFICATIONS

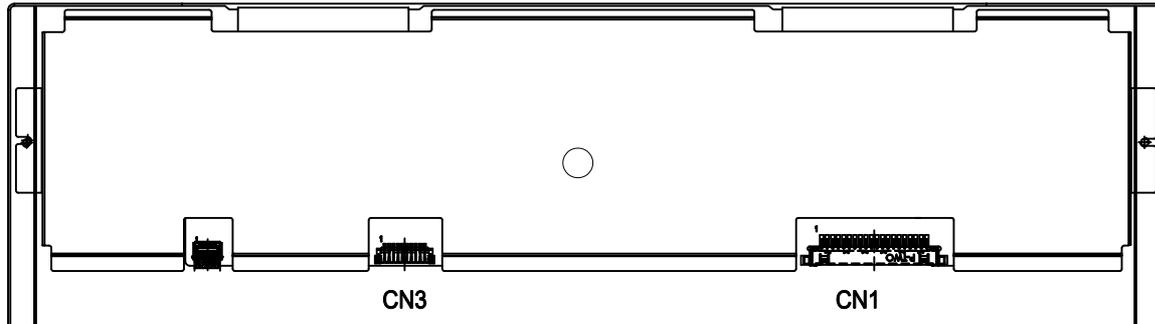
| Item | Description | Unit |
|------------------------------------|--|------|
| Display Size | 12.1 | inch |
| Display Type | Transmissive, a-Si | - |
| Active Area (HxV) | 245.76 (H) x 184.32 (V) | mm |
| Number of Dots (HxV) | 1024 x RGB x 768 | dot |
| Pixel Pitch (HxV) | 0.08 x 0.08 | mm |
| Color Arrangement | RGB Stripe | - |
| Color Numbers | 256K/16.7 M | - |
| Outline Dimension (HxVxT) | 260.5 (H) x 204 (V) x 8.51 (D) | mm |
| White Point (x,y) (Underlight) | x:0.305,y: 0.337 (Typ.) | |
| Response Time | ≤ 35 | ms |
| Viewing Angle (Light On) (R/U/L/D) | Cr ≥ 10 @ R/L/U/D (85°/85°/85°/85°) (Min.) | |
| Surface Treatment | AG | |
| Contrast Ratio (Light On) | 1000:1 (Typ) | |
| Operation Temperature | -30~80 | °C |
| Storage Temperature | -30~80 | °C |
| Interface | LVDS | |
| Weight | 569 (Typ) | g |
| Panel power consumption | Max:(1.66W)@white pattern | W |

3. PIN DESCRIPTION

3.1 Connector

There are 4 connectors on PCBA, location & Pin1 is showed on below figure.

BACK View



Connectors' type:

1. CN1 : Input LVDS CONN,20pins, P-TWO 187191-20101-3
2. CN3: Input BL power CONN,10pins, ACES, 91208-01001-H01

3.2 PIN assignment

3.2. 1 Connector 1 :

A 20pin connector of P-two 187191-20101-3 is used for the module electronics interface. And a special plug needed for connecting this connector, the recommended model is JAE FI-S20S.

Pin assignment:

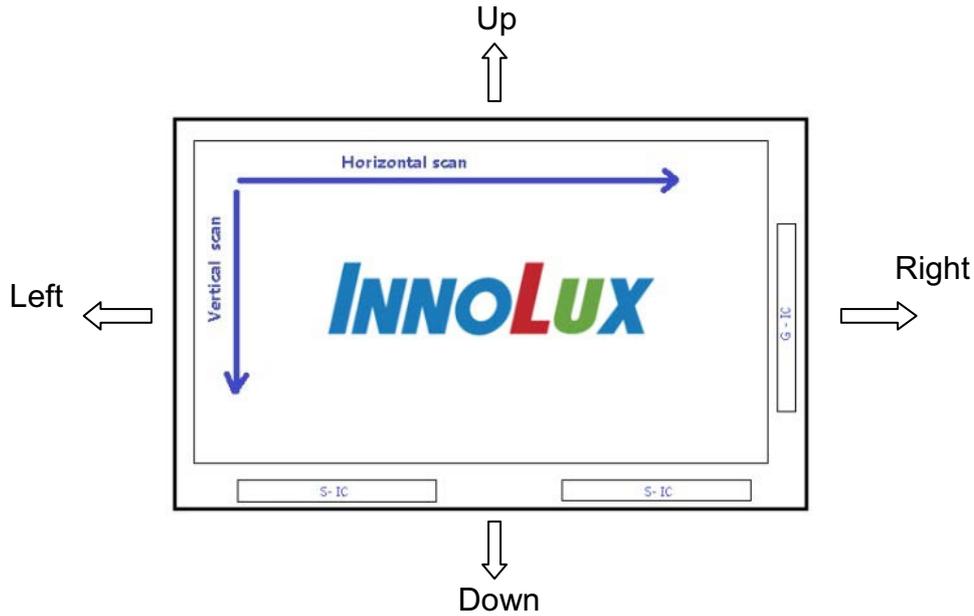
| Pin NO. | Symbol | Description | Note |
|---------|--------|---|------|
| 1 | RX3+ | Differential Data Input, CH3 (Positive) | |
| 2 | RX3- | Differential Data Input, CH3 (Negative) | |
| 3 | BIST | Normal operation/BIST pattern select BIST=0: Normal operation BIST=1: BIST mode | 1 |
| 4 | SEL68 | LVDS 6/8 bit select function control, SEL68=1: LVDS input data is 8 bit SEL68=0: LVDS input data is 6 bit | 2 |
| 5 | GND | Ground | |

| | | | |
|----|------|--|--------|
| 6 | RXC+ | Differential Clock Input (Positive) | |
| 7 | RXC- | Differential Clock Input (Negative) | |
| 8 | GND | Ground | |
| 9 | RX2+ | Diferential Data Input, CH2 (Positive) | |
| 10 | RX2- | Diferential Data Input, CH2 (Negative) | |
| 11 | GND | Ground | |
| 12 | RX1+ | Dif ferential Da& Input, CH1 (Positive) | |
| 13 | RX1- | Dif ferential Data Input, CH1 (Negative) | |
| 14 | GND | Ground | |
| 15 | RX0+ | Differential Data Input, CH0 (Positive) | |
| 16 | RX0- | Dif ferential Data Input, CH0 (Negative) | |
| 17 | reLR | Left or right display control LR=1: Left-->Right LR=0: Right--> Left | Note 3 |
| 18 | reUD | Up or Down display control LR=1: Up-->Down LR=0: Down--> Up | Note 3 |
| 19 | VDD | Power supply. 3.3V | |
| 20 | VDD | Power supply. 3.3V | |

Note:

- Pin1 is reversed as BIST function for test, don't connect signal to this pin, keep floating.
- SEL68 is used for selecting 6bit/8bit LVDS data input, **1: connect to VDD -->8bit; 0: connect to GND-->6bit.**
- reLR & reUD are used for selecting scanning direction.0: connect to GND; 1: connect to VDD.

| Setting of scan control input | | Scanning direction |
|-------------------------------|------|---------------------------|
| reLR | reUD | |
| 1 | 1 | left to right ,up to down |
| 1 | 0 | left to right, down to up |
| 0 | 1 | right to left ,up to down |
| 0 | 0 | right to left ,down to up |

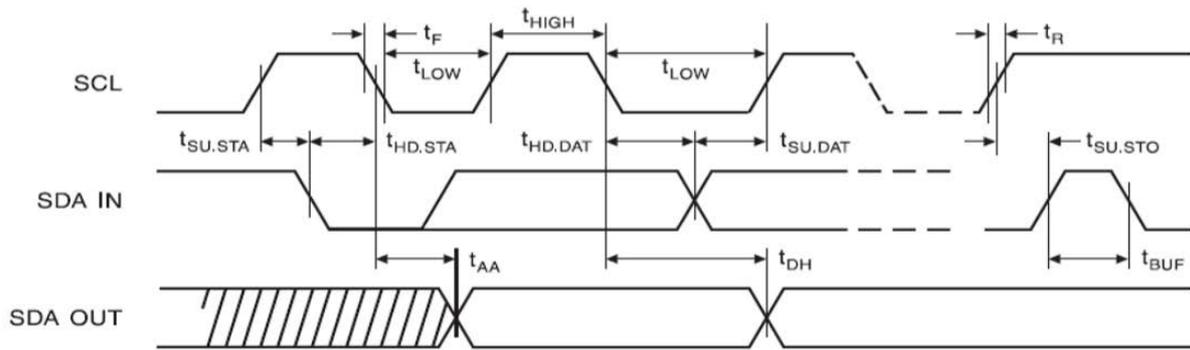


Note1: I2C DC/AC CHARACTERISTICS as following.

| I2C INTERFACE---SDA,SCL,A0,WPN | | | | | | |
|--|--------------|--------------------------------------|-----|-----|------|------------|
| Low Level Input Voltage | V_{IL} | VIN=2.5V to 5.5V | 0 | | 0.8 | V |
| High Level Input Voltage | V_{IH} | VIN=2.5V to 5.5V | 1.5 | | 5.5 | V |
| SDA, SCL Hysteresis | | | 0.6 | 0.7 | 0.8 | V |
| Internal Pull High Resistor | R_{PULL-1} | A0 internal pull high(VIN1) resistor | 8 | 10 | 12 | K Ω |
| EEPROM Write Protect | | When WPN = High, can't write EEPROM | 1.5 | | 5.5 | V |
| EEPROM Write Time | T_{WRITE} | | 30 | | 500 | msec |
| Number of Guaranteed EEPROM Write Cycles | N_{WRITE} | | 1 | | 1000 | Cycles |

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------|--|------|------|------|------|
| F_{SCL} | Clock Frequency, SCL | 0 | - | 400 | kHz |
| t_{LOW} | Clock Pulse Width Low | 1.3 | - | | us |
| t_{HIGH} | Clock Pulse Width High | 0.6 | - | | us |
| t_1 | Noise Suppression Time(2) | | | 10 | ns |
| t_{BUF} | Time the bus must be free before a new transmission can start(2) | 1.3 | | | us |
| $t_{HD,STA}$ | Start Hold Time | 0.6 | | | us |
| $t_{SU,STA}$ | Start Setup Time | 0.6 | | | us |
| $t_{HD,DAT}$ | Data In Hold Time | 0 | | 900 | ns |
| $t_{SU,DAT}$ | Data In Setup Time | 100 | | | ns |
| t_R | Inputs Rise Time(2) | | | 1 | us |
| t_F | Inputs Fall Time(2) | | | 300 | ns |
| $t_{SU,STO}$ | Stop Setup Time | 0.6 | | | us |
| t_{AA} | Clock Low to Data Out Valid | 0.1 | | 0.9 | us |
| t_{DH} | Data Out Hold Time | 50 | | | ns |

I2C Bus Timing



Note 2: 0TP D-VCOM adjust flow as Appendix 1

3.2.3 Connector 3 : Input BL power CONN

CONN type: ACES, 91208-01001-H01 the recommended male connector is ACES:50216-01011-001 or equivalent.

10-pin connector pin assignment:

| Pin NO. | Symbol | Description |
|---------|----------|--|
| 1 | LED_VCCS | LED convertor input power, 12V |
| 2 | LED_VCCS | LED convertor input power, 12V |
| 3 | LED_VCCS | LED convertor input power, 12V |
| 4 | LED_VCCS | LED convertor input power, 12V |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | GND | Ground |
| 9 | LED_EN | Converter power IC output Enable (Active High) |
| 10 | LED_PWM | PWM control signal for LED convertor |

4. ABSOLUTE MAXIMUM RATING

| Item | Symbol | Min. | Max. | Unit | Remark |
|-----------------------|----------|------|------|------|--------|
| Power Supply Voltage | VDD | -0.3 | 3.8 | V | |
| | LED_VCCS | -0.3 | 25 | V | |
| Storage Temperature | Tstg | -30 | +80 | °C | |
| Operating Temperature | Topr | -30 | +80 | °C | |

Note:

- (1) All of the voltages listed above are with respect to GND= 0V
- (2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. DC CHARACTERISTICS

5.1 Parameter

| Item | Symbol | Values | | | Unit | Remark |
|---------------------------|-----------------------|--------|------|--------|------|---|
| | | Min. | Typ. | Max. | | |
| Power voltage | VDD | 3.0 | 3.3 | 3.6 | V | |
| | LED_VCCS | 11 | 12 | 13 | V | |
| Input logic high voltage | V _{IH} | 0.7VDD | - | VDD | V | 1 |
| Input logic low voltage | V _{IL} | 0 | - | 0.3VDD | V | |
| Current for Power | I _{VDD} | | - | (410) | mA | VDD =3.3V@frame 60 Hz, Whitepattern |
| | I _{LED_VCCS} | (400) | - | (425) | mA | LED_VCCS=12V, PWM Duty =100%, @ (8S4P) |
| | | (600) | | (635) | mA | LED_VCCS=12V, PWM Duty =100%, @ (11S4P) |
| LED_EN Control Level | BL On | 3.0 | - | 5 | V | |
| | BL Off | 0 | - | 0.3 | V | |
| LED_PWM Control Level | PWM High Level | 3.0 | - | 5 | V | |
| | PWM Low Level | 0 | - | 0.3 | V | |
| LED_PWM Control Frequency | f _{PWM} | 1K | - | 20K | Hz | 2 |

Note 1 : Including signal: SEL68 & reLR & reUD

Note 2: LED_PWM duty >10%.

5.2 LB power output

| Item | Symbol | Values | | | Unit | Remark |
|--------------|--------|--------|------|------|------|------------------|
| | | Min. | Typ. | Max. | | |
| Output Power | LED+ | 35 | 36 | 37 | V | LED+ =36V @12S4P |

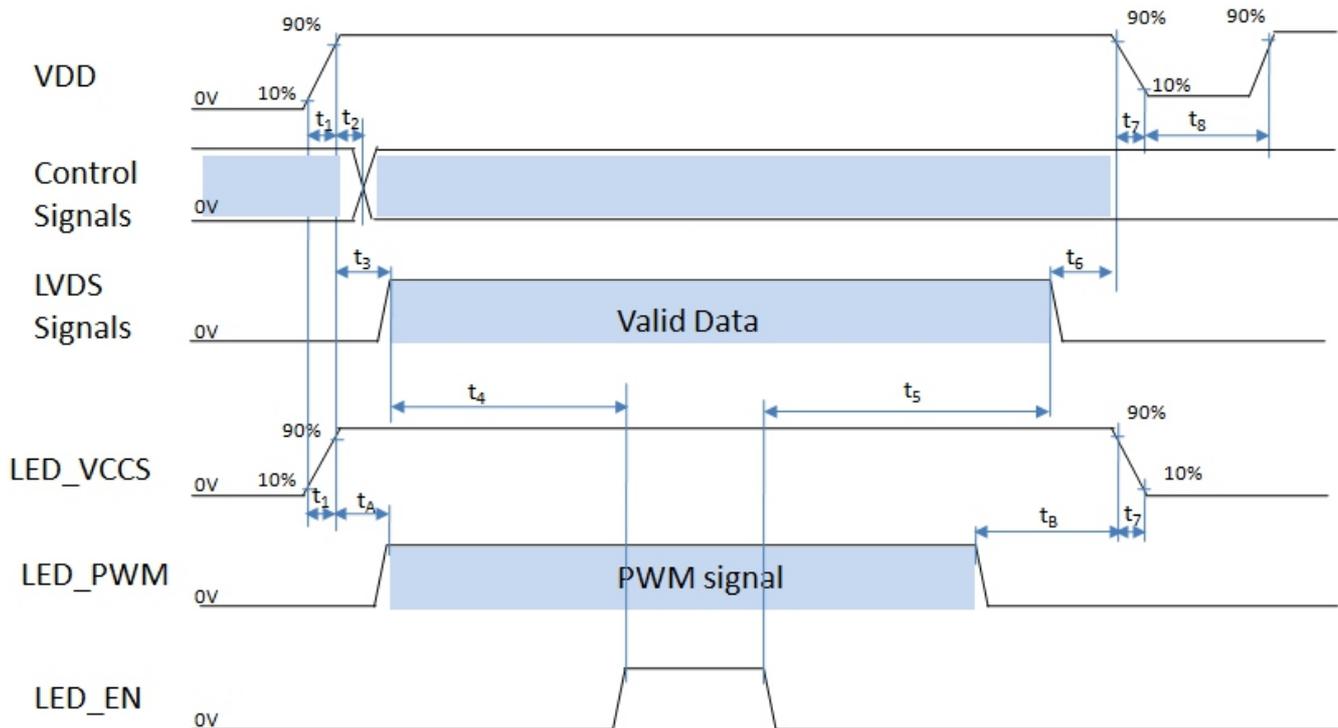
| | | | | | | |
|----------------------|-----------------|-------|----|-------|----|------------------------------------|
| Output Power Current | $I_{LED1+LED4}$ | 44.55 | 45 | 45.45 | mA | Total 180mA(Typ.)(45mA x 4channel) |
|----------------------|-----------------|-------|----|-------|----|------------------------------------|

Note 1: output power LED+ OVP is 40V.

5.3 Power sequence

The power sequence specifications are shown as the following table and diagram.

| Symbol | Value | | Unit |
|--------|-------|------|------|
| | Min. | Max. | |
| t_1 | 1 | 20 | ms |
| t_2 | 1 | 5 | ms |
| t_3 | 10 | 50 | ms |
| t_4 | 200 | 500 | ms |
| t_5 | 200 | 500 | ms |
| t_6 | 50 | 200 | ms |
| t_7 | 0 | 20 | ms |
| t_8 | 500 | - | ms |
| t_A | 0 | 50 | ms |
| t_B | 0 | 50 | ms |



Note 1: Please don't plug the interface cable of on when system is turned on.

Note 2: Please avoid floating state of the interface signal during signal invalid period.

Note 3: It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

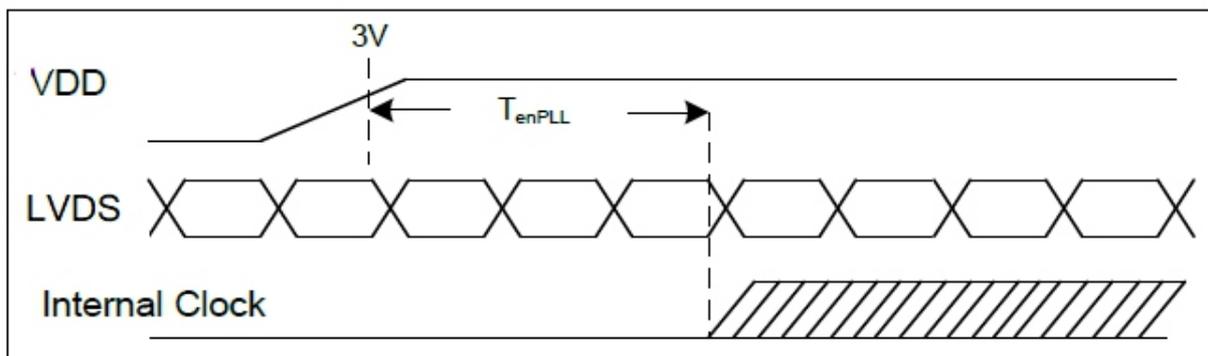
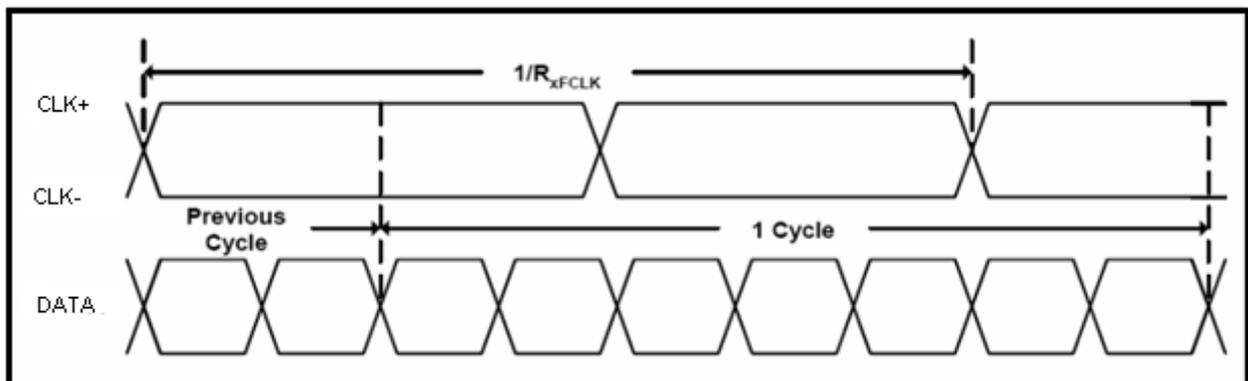
Note 4: Control signals include BIST, SEL68 , reUD & reLR.

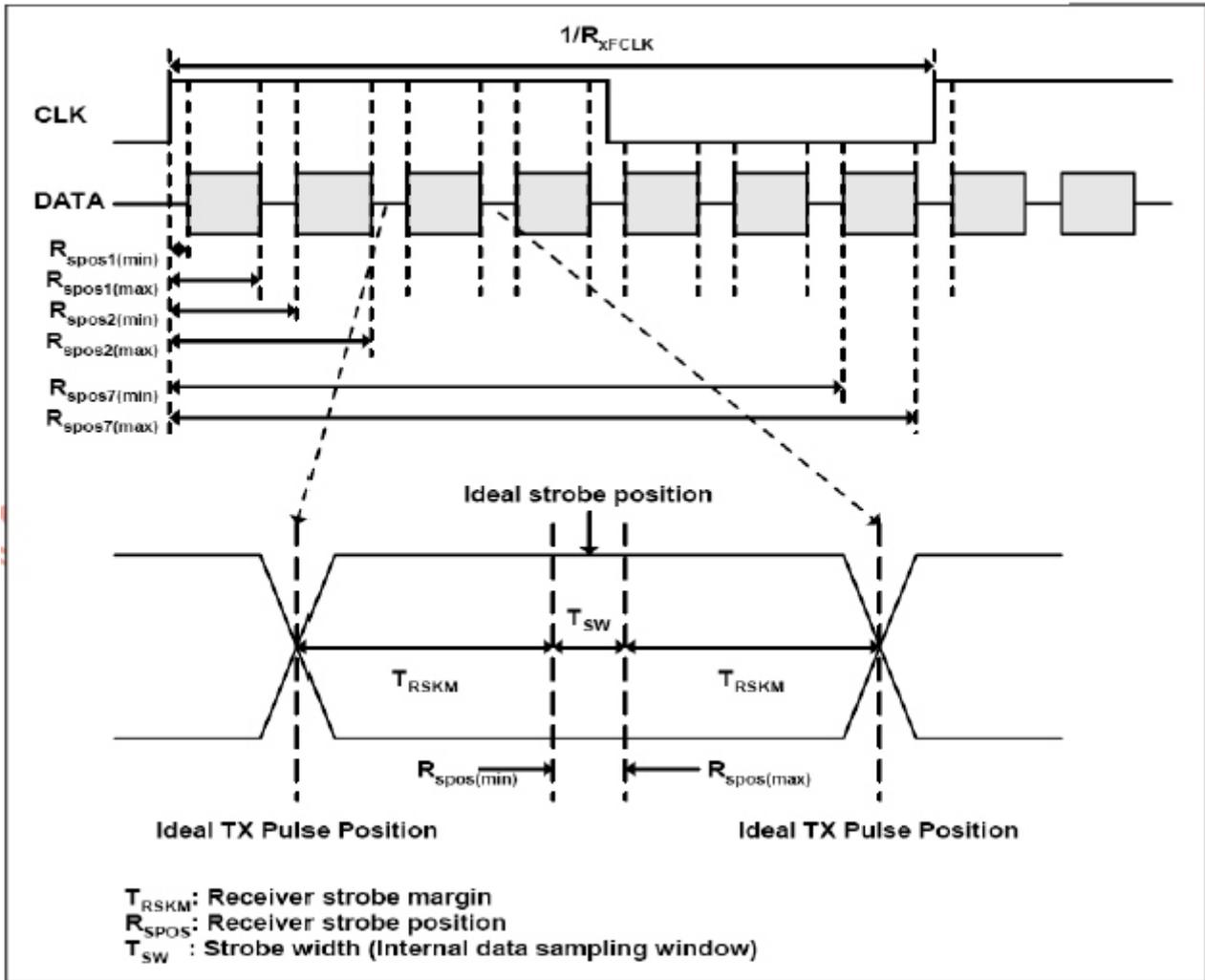
6. LVDS SIGNAL TIMING CHARACTERISTICS

6.1AC Electrical characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Condition |
|------------------------|--------|------|-----------------------|-----|-------|--|
| Clock frequency | RxFCLK | 26.2 | - | 71 | MHz | |
| Input data skew margin | TRSKM | 500 | - | - | ps | VID = 400mV RxVCM=1.2V RxFCLK=71MHz |
| Clock high time | TLVCH | - | $4/(7 \times RxFCLK)$ | - | ns | |
| Clock low time | TLVCL | - | $3/(7 \times RxFCLK)$ | - | ns | |
| PLL wake-up time | TenPLL | - | - | 150 | us | |

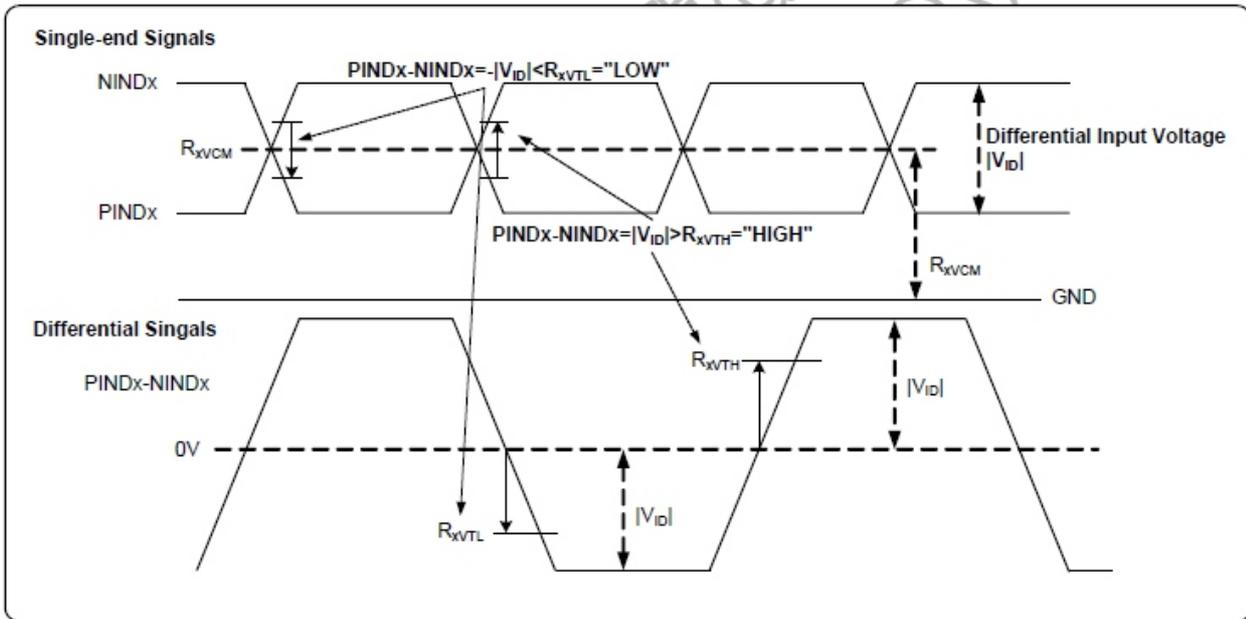
6.2 Input clock and data timing diagram





6.3 DC electrical characteristics

| Parameter | Symbol | Values | | | Unit | Remark |
|--|------------|-----------|------|---------------|------|-----------------|
| | | Min. | Typ. | Max. | | |
| LVDS Differential input high Threshold voltage | R_{xVTH} | - | - | +100 | mV | $R_{xVCM}=1.2V$ |
| LVDS Differential input low Threshold voltage | R_{xVTL} | -100 | - | - | mV | |
| Input Voltage range (Singed-end) | R_{xVIN} | 0 | - | 2.4 | V | |
| LVDS Differential input common mode voltage | R_{xVCM} | $ V_D /2$ | - | $2.4- V_D /2$ | V | |
| LVDS Differential input voltage | $ V_D $ | 0.2 | - | 0.6 | V | |

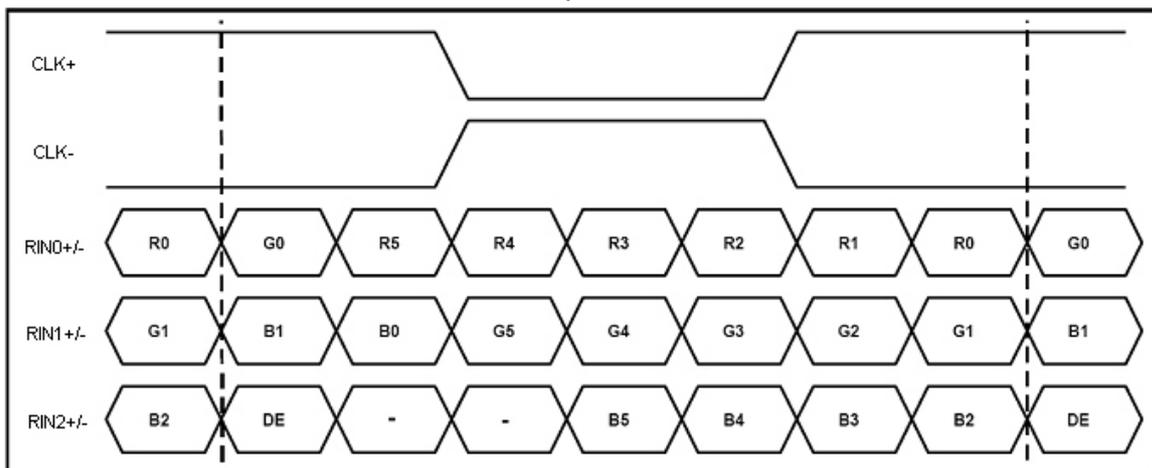


6.4 data timing

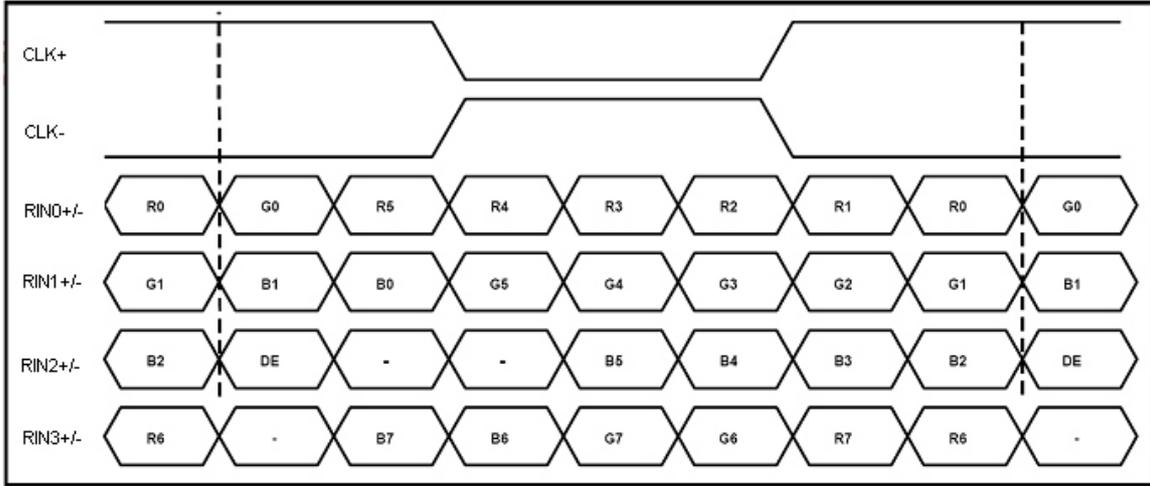
| Parameter | Symbol | Spec. | | | Unit |
|-------------------------|-----------|-------|------|------|-------|
| | | Min. | Typ. | Max. | |
| DCLK frequency | fclk | 52 | 65 | 71 | MHz |
| Horizontal display area | thd | 1024 | | | DCLK |
| HSD period | th | 1114 | 1344 | 1400 | DCLK |
| HSD blanking | thb+thfp | 90 | 320 | 376 | DCLK |
| Vertical display area | tvd | 768 | | | T_H |
| VSD period | tv | 778 | 806 | 845 | T_H |
| VSD blanking | tvbp+tvfp | 10 | 38 | 77 | T_H |

6.5 LVDS data input format

SEL68 = "Low" for 6 bits LVDS Input



SEL68 = "High" for 8 bits LVDS Input



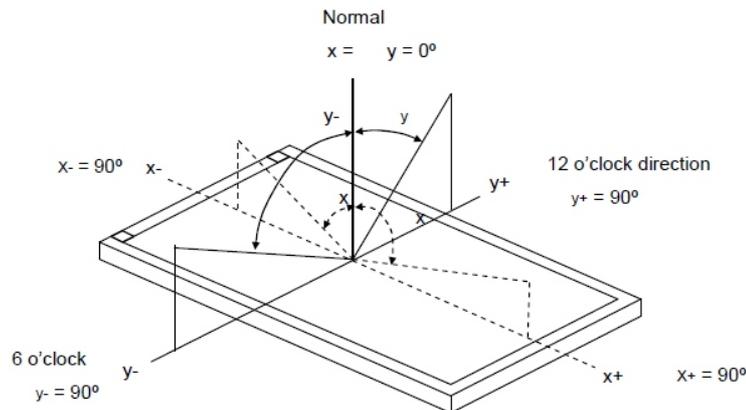
7. OPTICAL CHARACTERISTICS

7.1 Optical specification

The relative measurement methods of optical characteristics are shown

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|-------------------------------|------------|--------------------------------|---|---------------|-------|---------------|-------------------|--------------------------------------|
| Color Chromaticity (CIE 1931) | White | W _x | q _x =0°, q _y =0° R=G=B=255 Gray scale | Typ - 0.03 | 0.305 | Typ + 0.03 | - | C Light Source (5) (6) (7) (8) |
| | | W _y | | | 0.327 | | | |
| Luminance uniformity | | YU | | 75 | - | - | % | |
| Luminance | | L | | 1000 | 1200 | - | cd/m ² | |
| Contrast Ratio | | CR | 700 | 1000 | - | - | (2) | |
| Response Time | | T _R +T _F | q _x =0°, q _y =0° | - | 25 | 35 | ms | (3) |
| NTSC (CIE1931) | | | (Under C light) | | 70 | | % | |
| Life Time | | | defined as the module brightness decrease to 50% original brightness at Ta=25 C | 50000 | - | - | Hrs | |
| Viewing Angle | Horizontal | X+ | CR ≥ 10 | 85 | 89 | - | Deg. | (1)(5) |
| | | X- | | 85 | 89 | - | | |
| | Vertical | Y+ | | 85 | 89 | - | | |
| | | Y- | | 85 | 89 | - | | |

Note (1) Definition of Viewing Angle (x, y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L₂₅₅: Luminance of gray level 255

L₀: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

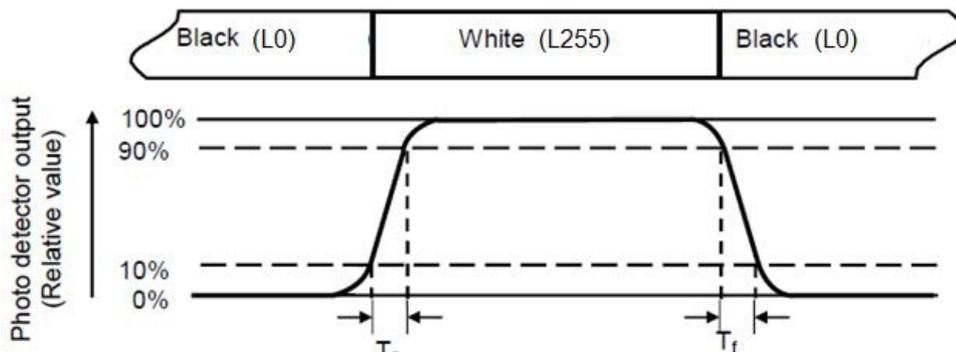
Note (3) Definition of Response Time

The response time is defined as the LCD optical switching time interval between 'White' state and 'Black' state. Rise time (Tr) is the time between photo detector output intensity changed from 10%

to 90%. And fall time (Tf) is the time between photo detector output intensity changed from 90% to 10%.

RT = RT (5)

RT (X) is corresponding to the Response Time of the point X at Figure in Note (6).



Note (4) Definition of Luminance of White (Lc)

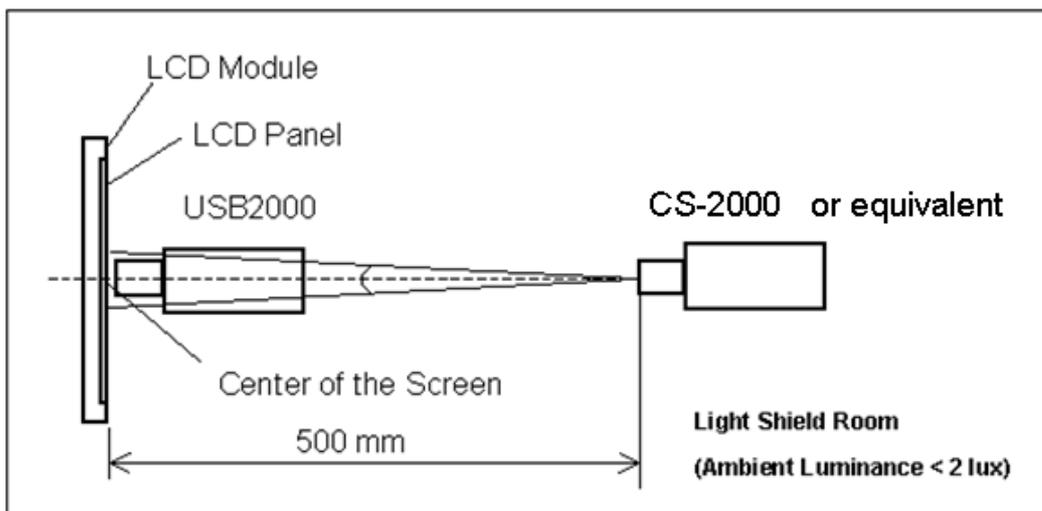
Measure the luminance of gray level 255 at center point

LC = L (5)

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 40 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room.



Note (6) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

All input terminals LCD panel must be ground while measuring the center area of the panel.

Note (7) Definition of color gamut (C.G%):

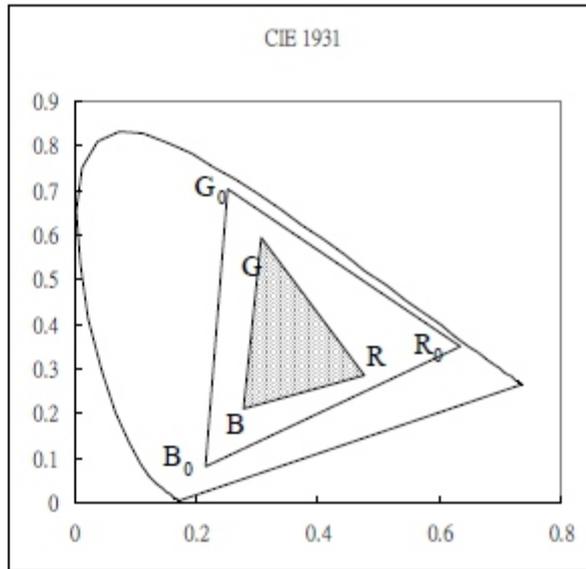
C.G%= RGB / R0 G0 B0, *100%

R₀, G₀, B₀: color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 255 gray levels of red, green, and blue, respectively.

R₀ G₀ B₀: area of triangle defined by R₀, G₀, B₀

R G B: area of triangle defined by R, G, B



Note 8:Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(Yu) = \frac{B_{\min}}{B_{\max}}$$

L-----Active area length W----- Active area width

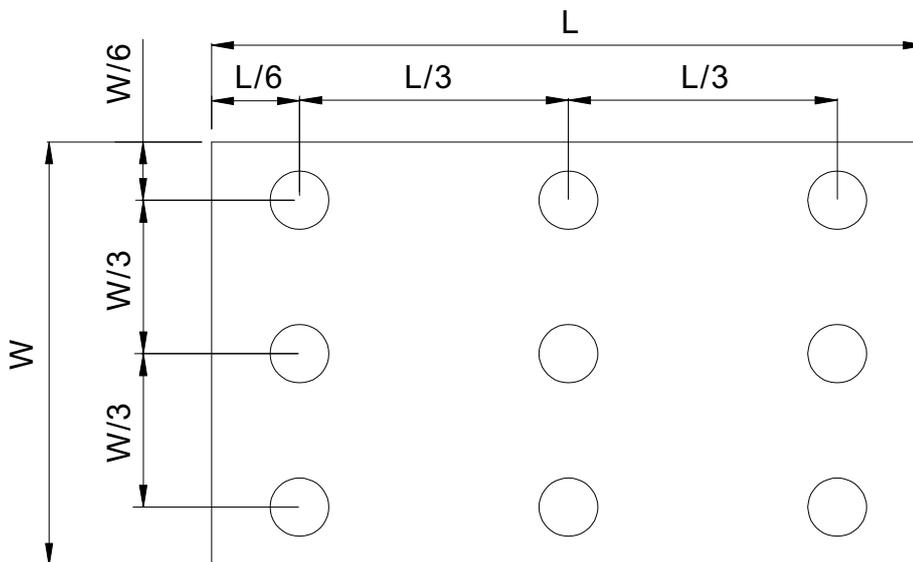


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement poition.

B_{min}: The measured minimum luminance of all measurement poition.

8. QUALITY ASSURANCE

| No. | Test Items | Test Condition | Note |
|-----|--|--|-----------|
| 1 | High Temperature Storage | 80℃, 240hrs | Note 1, 2 |
| 2 | Low Temperature Storage | -30℃, 240hrs | Note 1, 2 |
| 3 | High Temperature Operation | 80℃, 240hrs | Note 1, 2 |
| 4 | Low Temperature Operation | -30℃, 240hrs | Note 1, 2 |
| 5 | High Temperature and High Humidity Storage | 60℃, 90%RH, 240hrs | Note 1, 2 |
| 6 | Thermal Shock | -30℃/0.5h ~ +80℃/0.5h for a total 100 cycles | Note 1, 2 |

Note 1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.

Note 2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

Note 3 : Under no condensation of dew.

9. PRECAUTIONS

9.1 ESD (Electrical Static Discharge) strategy

- [1] ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy
- [2] In handling LCD panel, please wear gloves with non-charged material. Using the conduction ring connects wrist to the earth and the conducting shoes to the earth necessary is.
- [3] The machine and working table for the panel should have ESD protection strategy.
- [4] In handling the panel, ionized airflow decreases the charge in the environment is necessary.
- [5] In the process of assemble module, shield case should connect to the ground.

9.2 Environment

- [1] Working environment of the panel should be in the clean room.
- [2] Because touch panel has protective film on the surface, please remove the protection film slowly with ionized air to prevent the electrostatic discharge.

9.3 Assembly and handling precautions

- [1] Do not apply improper or unbalanced force such as bending or twisting to open cells during assembly.
- [2] It is recommended to assemble or to install an open cell into a customer's product in clean working areas. The dust and oil may cause electrical short to an open cell or worsen polarizers on an open cell.
- [3] Do not apply pressure or impulse to an open cell to prevent the damage.
- [4] Always follow the correct power-on sequence when an open cell is assembled and turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] Do not design sharp-pointed structure / parting line / tooling gate on the plastic part of a COF (Chip on film), because the burr will scrape the COF.
- [6] If COF would be bended in assemble process, do not place IC on the bending corner.
- [7] The gap between COF IC and any structure of BLU must be bigger than 2 mm. This can prevent the damage of COF IC.
- [8] The bezel opening must have no burr and be smooth to prevent the surface of an open cell scraped.
- [9] The bezel of a module or a TV set can not contact with force on the surface of an open cell. It might cause light leakage or scrape.
- [10] In the case of no FFC or FPC attached with open cells, customers can refer the FFC / FPC drawing and buy them by self.

- [11] It is important to keep enough clearance between customers' front bezel/backlight and an open cell. Without enough clearance, the unexpected force during module assembly procedure may damage an open cell.
- [12] Do not plug in or unplug an I/F (interface) connector while an assembled open cell is in operation.
- [13] Use a soft dry cloth without chemicals for cleaning, because the surface of the polarizer is very soft and easily scratched.
- [14] Moisture can easily penetrate into an open cell and may cause the damage during operation.
- [15] When storing open cells as spares for a long time, the following precaution is necessary.
- [15.1] Do not leave open cells in high temperature and high humidity for a long time. It is highly recommended to store open cells in the temperature range from 0 to 35 at normal humidity without condensation.
- [15.2] Open cells shall be stored in dark place. Do not store open cells in direct sunlight or fluorescent light environment.
- [16] When ambient temperature is lower than 10°C, the display quality might be reduced.
- [17] Unpacking (Cartons/Tray plates) in order to prevent open cells broken:
- [17.1] Moving tray plates by one operator may cause tray plates bent which may induce open cells broken. Two operators carry one carton with their two hands. Do not throw cartons/tray plates, avoid any impact on cartons/tray plates, and put down & pile cartons/tray plates gently.
- [17.2] A tray plate handled with unbalanced force may cause an open cell damaged. Trays should be completely put on a flat platform.
- [17.3] To prevent open cells broken, tray plates should be moved one by one from a plastic bag.
- [17.4] Please follow the packing design instruction, such as the maximum number of tray stacking to prevent the deformation of tray plates which may cause open cells broken.
- [17.5] To prevent an open cell broken or a COF damaged on a tray, please follow the instructions below:
- [17.5.1] Do not peel a polarizer protection film of an open cell of on a tray
- [17.5.2] Do not install FFC or LVDS cables of an open cell on a tray
- [17.5.3] Do not press the surface of an open cell on a tray.
- [17.5.4] Do not pull X-board when an open cell placed on a tray.
- [18] Unpacking (Hard Box) in order to prevent open cells broken:
- [18.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with

their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[18.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[18.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[18.3.1] Do not peel a polarizer protection film of an open cell of in a hard box.

[18.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[18.3.3] Do not press the surface of an open cell in a hard box.

[18.3.4] Do not pull X-board when an open cell placed in a hard box.

[19] Handling – In order to prevent open cells, COFs , and components damaged:

[19.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[19.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[19.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[19.4] Handle open cells one by one.

[20] Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

9.4 Lamination precautions

[1] Air-Bonding the touch panel or cover is recommended instead of OCA/OCR full lamination.

9.5 Safety precautions

[1] If the liquid crystal material leaks from the open cell, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[2] After the end of life, open cells are not harmful in case of normal operation and storage.

9.6 Others

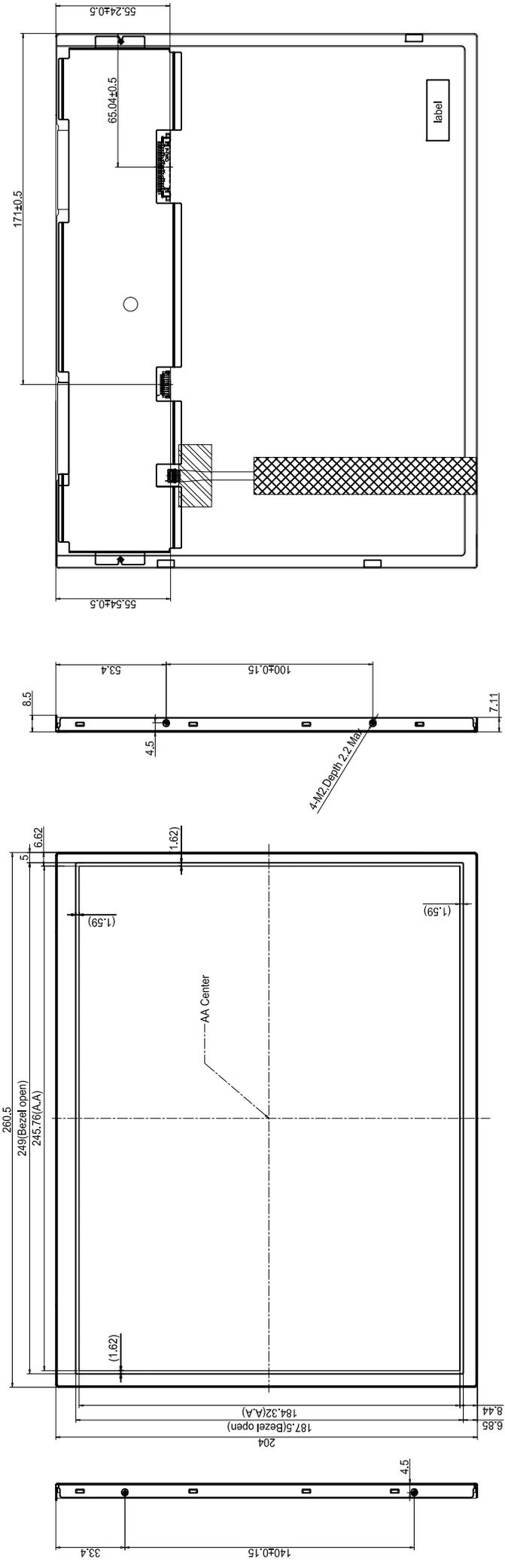
[1] Turn of the power supply before connecting and disconnecting signal input cable.

[2] Because the connection area of FPC and panel is not so strong, do not handle panel only by FPC or bend FPC.

- [3] Water drop on the surface or condensation as panel power on will corrode panel electrode.
- [4] As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
- [5] In the case the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hands cleanly with water and soap as soon as possible.

MECHANICAL OUTLINE, UNIT:mm
(Unspecified Tolerances is: ±0.3 mm)

10. MECHANICAL DRAWING

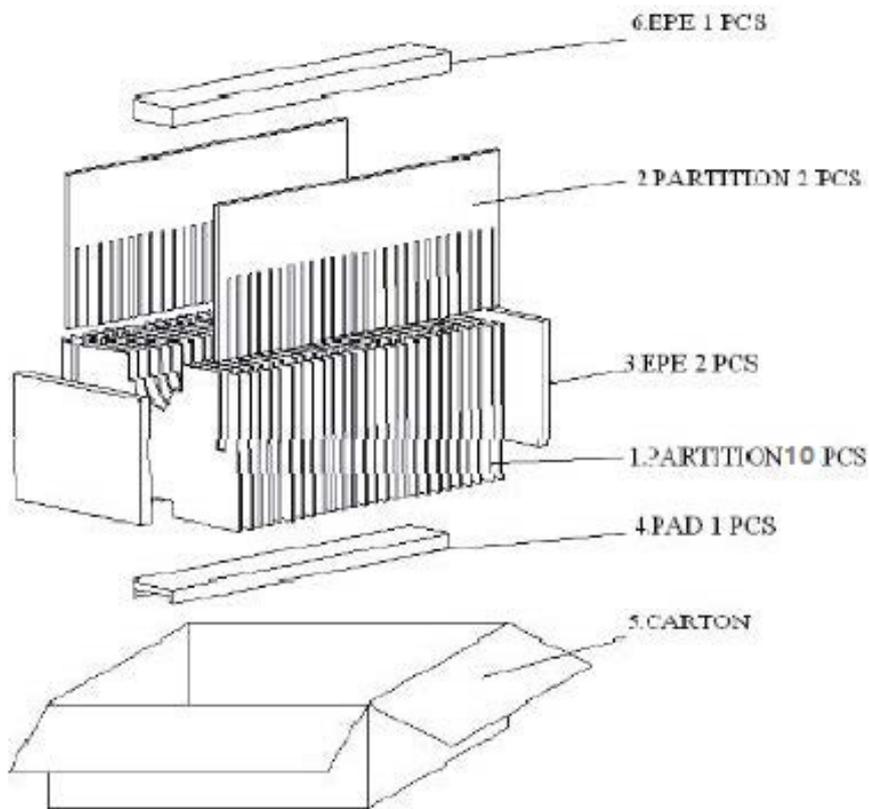


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|---------|------|--------------|------|---------|
| Version | Mark | Modification | Date | Made by |
| V1.0 | | | | |

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|-------------|----------|--------------|----------|
| DESIGN | MODEL | CLASS | REVISION |
| REVIEW | MATERIAL | FIRST DESIGN | DATE |
| APPROVAL | NO. | PAGE:1 | TOTAL:1 |
| 厦门炬盛森科技有限公司 | | | |

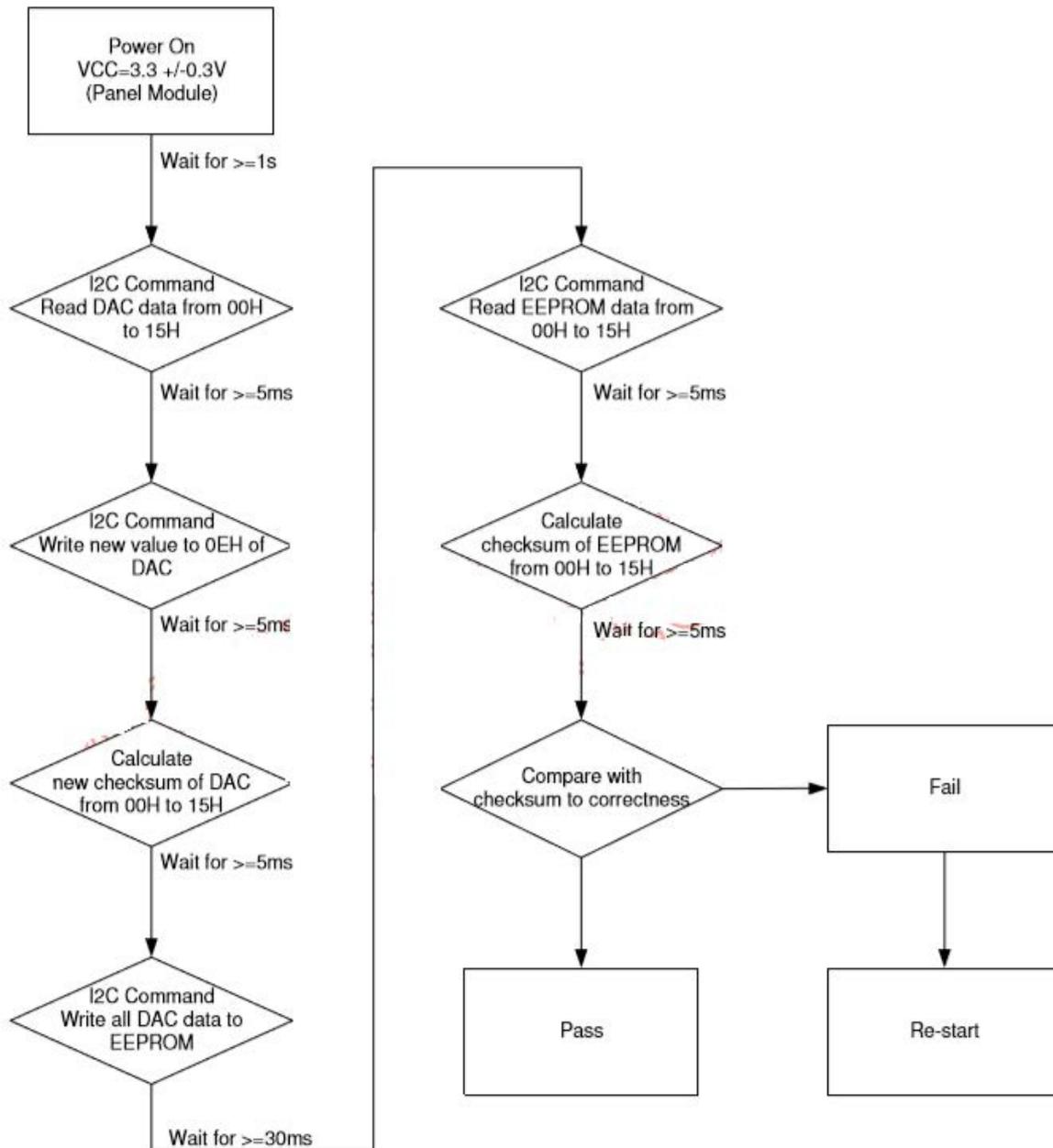
11. PACKING DRAWING

| LCM Model | Qty. in the Box | Box Size(mm) | Notes |
|------------|-----------------|-----------------------------------|-------|
| VI121VIC00 | 18pcs/Box | Ref. 375 x 355 x 300 ^H | |



Appendix 1

1.1 OTP D-VCOM adjust flow



1.2. OTP D-VCOM I2C register address & setting

Please refer to IN512-NO03(Novatek) IC datasheet part I2C Command List and Description for D-VCOM I2C register address & setting description.